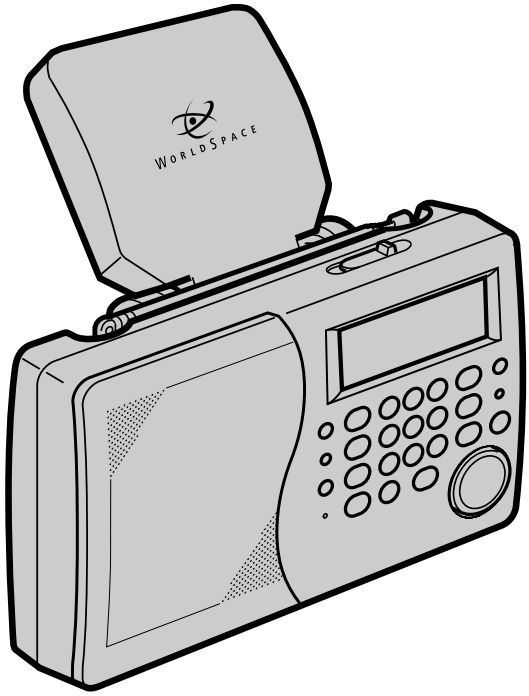
HITACHI

No. 0096E

KHWS1W
KHWS1WUN

SERVICE MANUAL



CONTENTS

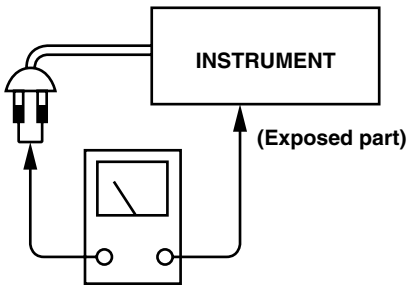
SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

DIGITAL RECEIVER

November 1999 HITACHI CONSUMER PRODUCTS (S)

Check that exposed parts are acceptably insulated from the supply circuit before returning the repaired instrument to the customer.

- **Checking method**
  Measure the resistance value between the both poles of attachment cup (Power supply plug) and the exposed parts (Parts such as Knob, Cover, etc. where the customer is easy to touch.) and check that the resistance value is 500 kohms or more.



Insulation tester (DC 500V)

SAFETY PRECAUTIONS

The following precautions should be observed when servicing.

1. Since many parts in the unit have special safety-related characteristics, always use genuine Hitachi's replacement parts. Especially critical parts in the power circuit block should not be replaced with other makers. Critical parts are marked with ⚠ in the circuit diagram and printed wiring board.
2. Before returning a repaired unit to the customer, the service technician must thoroughly test the unit to ascertain that it is completely safe to operate without danger of electrical shock.

SPECIFICATIONS

• WS (WorldSpace digital broadcast) Section

Circuit system:	Digital Receiver
Broadcast method:	WorldStar 1 Method
Receiver frequency:	L-Band (1453.384-1490.644 MHz)
Input/Output terminals	
Antenna input terminal	
Type/Impedance:	F-type/50 Ω
Polarization voltage:	LHCP 2.5-2.2 V RHCP 3.3-2.8 V
Max. current supply:	70 mA
External terminal:	9-pin, for future expansion
WS antenna (Built-in, detachable type):	WorldStar 1 Method compatible antenna Gain: over 6 dBi Dimensions: 150 x 33 x 156 mm (w x h x d)

• Radio Section

Circuit system:	FM/MW/SW1/SW2 4-bands Superheterodyne
Tuning range:	FM: 87.5 - 108 MHz MW: 522 - 1620 kHz (9 kHz steps) 520 - 1620 kHz (10 kHz steps) SW1: 2.300-7.300 MHz Meter band: 120, 90, 75, 60, 49, 41 m SW2: 9.500-26.100 MHz Meter band: 31, 25, 21, 19, 16, 13, 11 m
Antennas:	FM/SW1/SW2: Telescopic antenna (aerial) MW: Built-in ferrite-core antenna (aerial)

• General Specifications

Power supply:	AC: 110-127 V/220-240 V, 50/60 Hz DC: 6 V "D" cell or IEC R20 or equivalent x 4 (Optional) DC input jack Input voltage : DC 6 V + 30%, –10% (DC 7.8 V – 5.4 V) Current consumption: max. 400 mA
Power (mains) consumption:	5 W
Audio output:	3 W (PMPO) 300 mW (DC operation, 10% THD)
Speaker:	65 mm Cone/8 Ω
Output/Impedance:	Headphones (stereo)/ Suitable impedance: 8-100 Ω Line out (stereo)/2.2 kΩ
Battery life time:	30 hours over by using alkaline (LR20) batteries. 12 hours over by using manganic (R20P) batteries. (Use HITACHI battery/Measured method: EIAJ CP-2905A)
Dimensions:	240.5 x 162.5 x 64.5 mm 240.5 x 162.5 x 93 mm (w x h x d) (including the WS antenna and handle)
Weight:	1.5 kg (without batteries), 1.9 kg (with batteries)

• Accessories

AC power cord:	1
AC plug adaptor:	1
F-type connector:	1 set (for making an extention coaxial cable)
Waterproof cover:	1
Waterproof tape:	1

NOTE:

* Specifications are subject to change without notice.

SERVICE POINTS

1. Removal of Back Case (Fig. 1)
(1) Remove 3 screws ① from the back and 2 screws ② inside the battery compartment.
(2) Detach the Antenna from the Ant ⊙.
(3) Detach the connector Ⓐ.

2. Removal of SATELLITE P.W.B. Board (Fig. 2)
(1) Detach all connectors Ⓑ, Ⓒ and Ⓓ.
(2) Remove 1 screw ③ from the Satellite P.W.B. Board.
(3) Remove 2 screws ④ from the Satellite P.W.B. Board.
(4) Release the 3 catches and slide the Satellite P.W.B. Board away.

2. Removal of TUNER P.W.B. Board (Fig. 3)
(1) Detach 5 connectors Ⓔ, Ⓕ, Ⓖ, Ⓗ and Ⓘ from the Tuner P.W.B. Board.
(2) Turn to the opposite side, remove 1 screw ⑤ from the Tuner P.W.B. Board.
(3) Detach 9 catches and separate the Tuner P.W.B. Board from the sub-chassis.

3. Removal of Insulator Pad (Fig. 4)
(1) Remove 6 screws ⑤ from the Insulator pad.

4. Removal of Main Board (Fig. 5)
(1) Remove 4 screws ⑥ from the Main Board.

5. Removal of Speaker (Fig. 6)
(1) Release one end of the metal pin that secures the speaker position.
(2) Slide out the speaker.

6. Removal of POWER SUPPLY P.W.B. Board (Fig. 7)
(1) Remove 4 screws ⑦ and detach 1 connector Ⓙ from the Power Supply P.W.B. board.

7. Removal of ANTENNA P.W.B. Board (Fig. 7)
(1) Remove 1 screw ⑨ from the Antenna P.W.B. board.
(2) Gently pull the Antenna P.W.B. board outwards.

8. Removal of WS ANTENNA SUPPORT PLATE (Fig. 7)
(1) Remove the 6 screws ⑧ and pull the WS Antenna Support Plate away from the Back case.

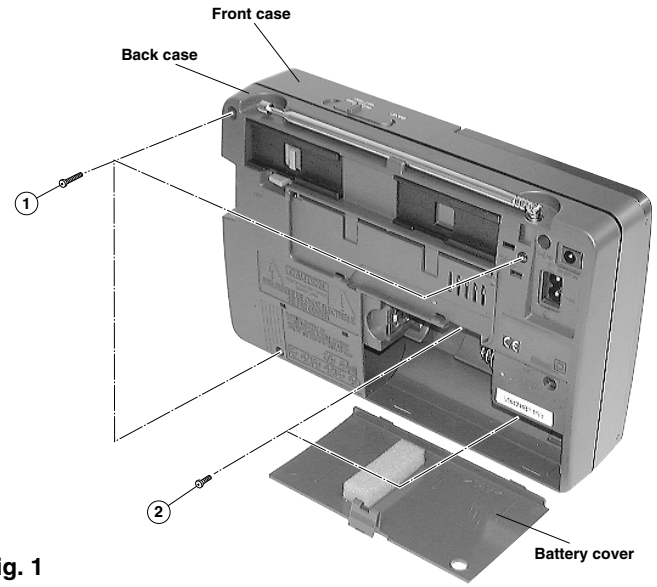


Fig. 1

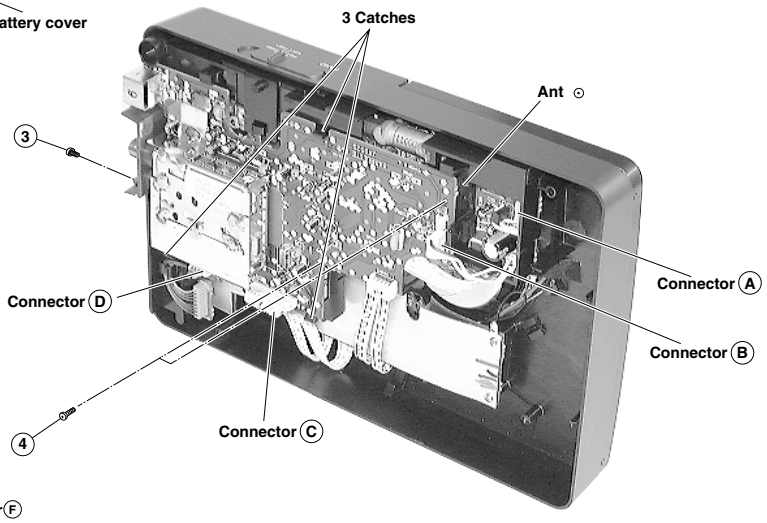


Fig. 2

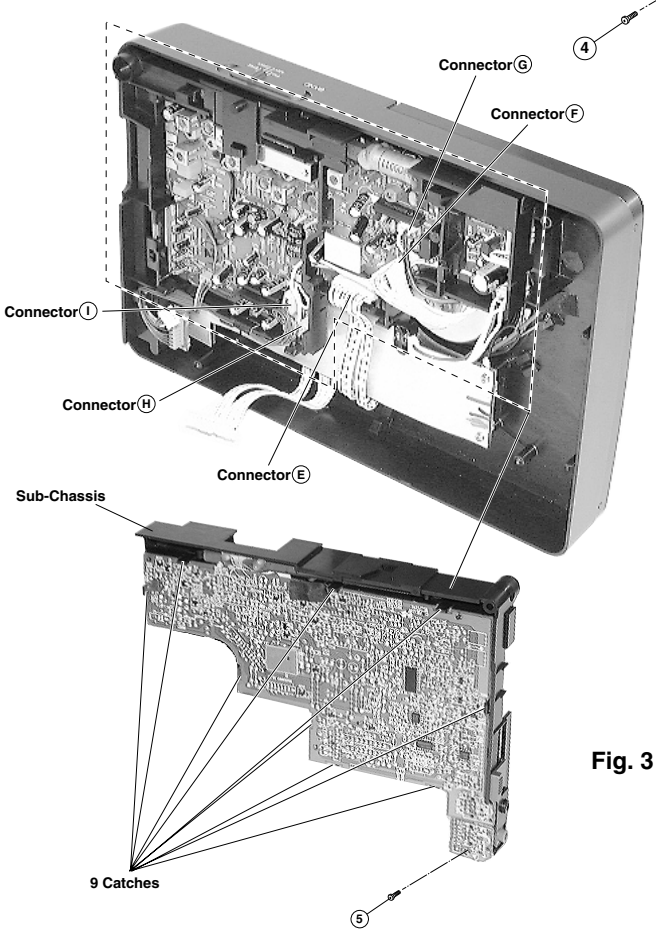


Fig. 3

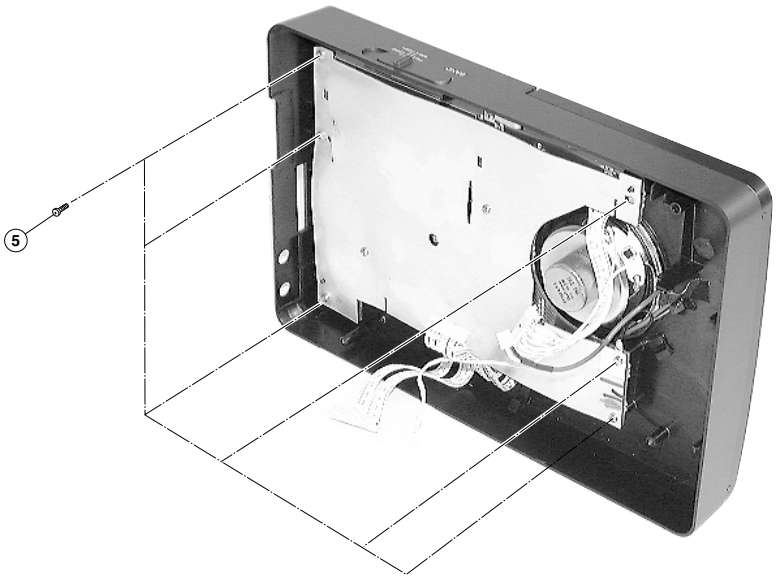


Fig. 4

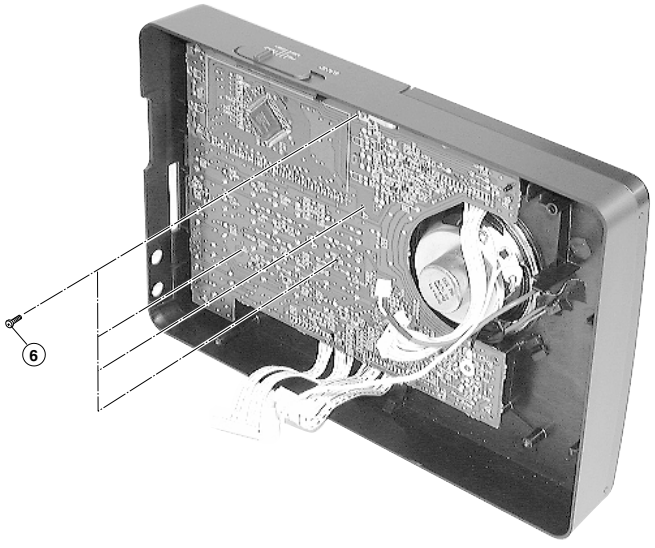


Fig. 5

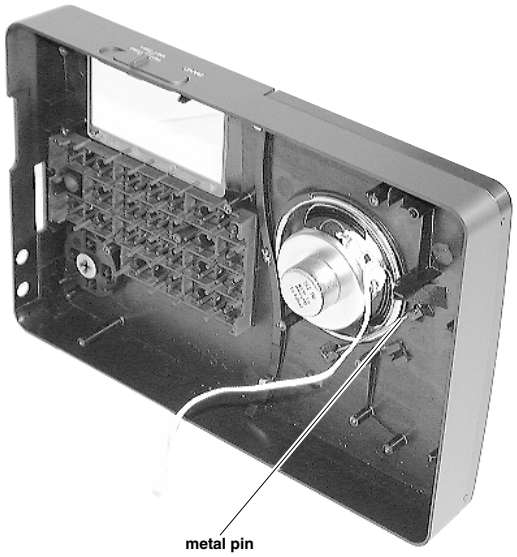


Fig. 6

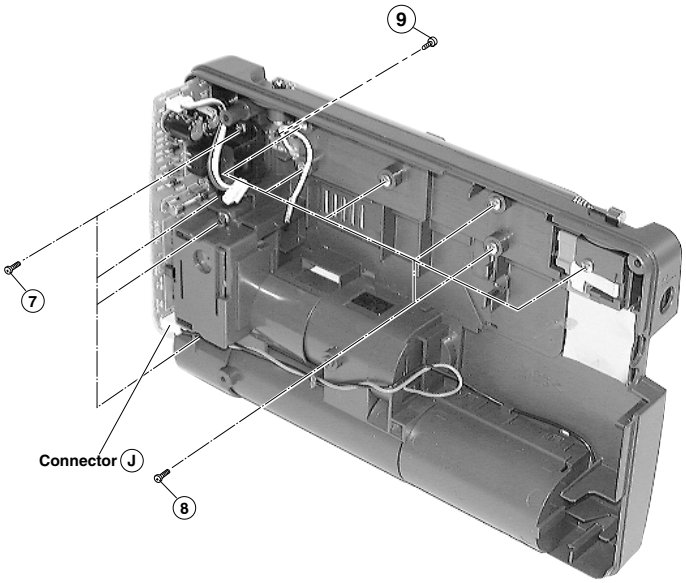
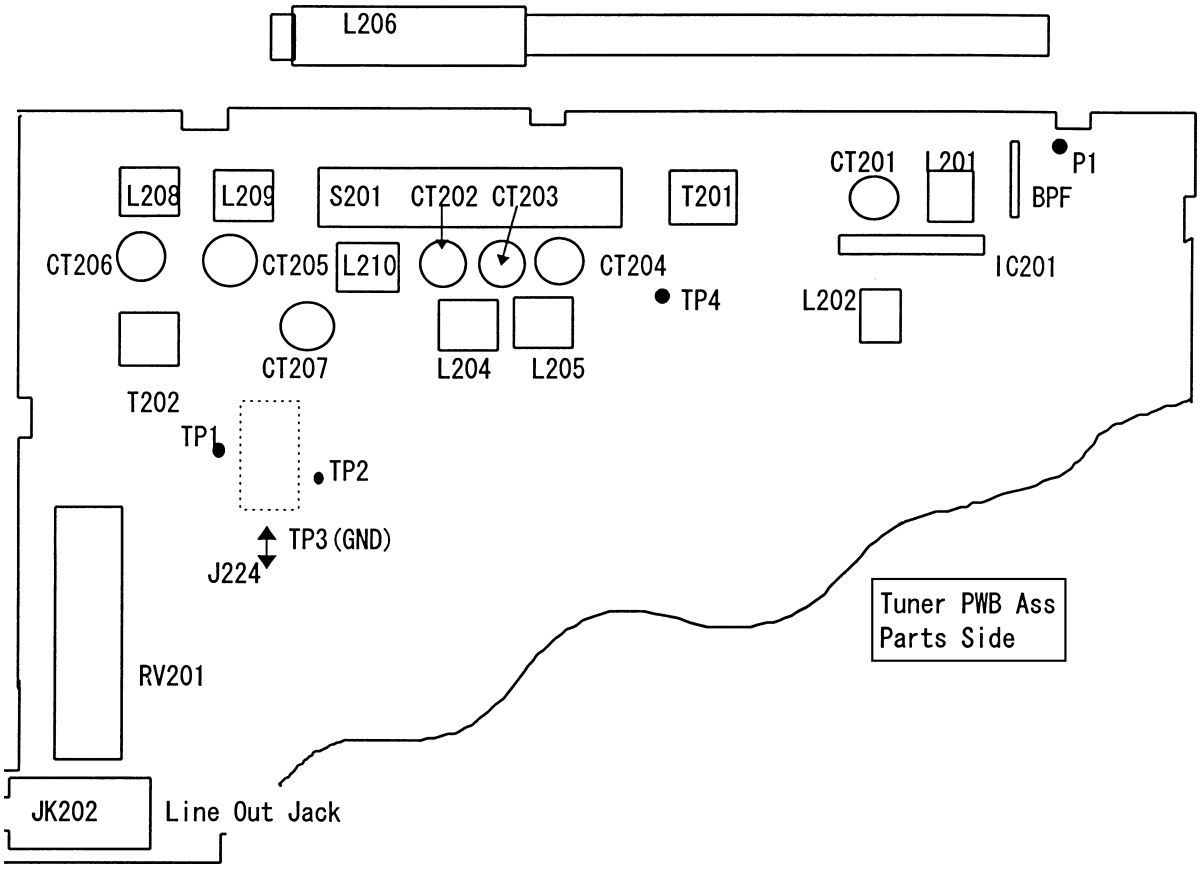


Fig. 7

ADJUSTMENTS

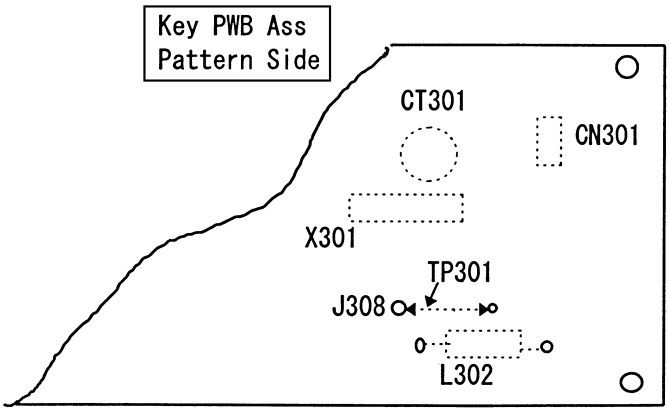
• Adjustment points (Must adjust RADIO Part only. Adjustment on WS Part is not necessary.)



Remarks:

* After adjustment, should be fix following parts by Electro Wax.
"L201, L202, L206"

* After adjustment, do not touch the alighed components. (especially L201 and L202)



• Adjustments

(1) Before Adjustment
1) Set the Power SW to ON.
2) Set the Radio Function.

(2) Alignment for Tuning Capacitor Voltage Range (Covering)
1) Required Instruments
* Signal Generator
* DC volt meter
2) Alignment Procedure
* Connect a DC Volt meter to TP4 (J201)

Band	Output Terminal	SG frequency & SET Tune	Adjustment	Reading
FM	TP4	87.5 MHz	L202	1.4 V ±0.1
		108 MHz	–	6 ~ 7.5 V
MW	TP4	1) 520 kHz (10 kHz step)/522 kHz (9 kHz step)	L210	1.2 V ±0.1
		2) 1620 kHz	CT207	7.2 V ±0.3
		3) Repeat step 1-2		
SW1	TP4	1) 2.3 MHz	L208	1.1 V ±0.1
		2) 7.3 MHz	CT205	8.8 V ±0.3
		3) Repeat step 1-2		
SW2	TP4	1) 9.5 MHz	L209	1.6 V ±0.1
		2) 26.1 MHz	CT206	9.0 V ±0.3
		3) Repeat step 1-2		

(3) Alignment for AM IF and MW, SW1, 2 Tracking

Step		Item	Required Instrument & Connection			Genescope or SG Freq.	Receiving Freq. (Set)	Adjust	Reading
			Instrument	Input	Output				
1		AM IF	Genescope (*1)	Ferrite Ant.*2	TP1	450 kHz	High end Freq.	T202	Max. Note 1
2	(1)	MW Ant	AM signal generator	F. Ant *2	TP1	600/603 kHz	600/603 kHz	L206	Max.
	(2)		400 Hz, 30% Mod.			1400/1404 kHz	1400/1404 kHz	CT204	
	(3)		ACVTM, oscillscope			Repeat steps (1) & (2)			
3	(1)	SW1 Ant	MW: Note 2	P1	TP1	3.2 MHz	3.2 MHz	L205	Max.
	(2)					7.1 MHz	7.1 MHz	CT203	
	(3)		SW1,2: Note 5			Repeat steps (1) & (2)			
4	(1)	SW2 Ant		P1	TP1	11.65 MHz	11.65 MHz	L204	Max.
	(2)					21.45 MHz	21.45 MHz	CT202	
	(3)					Repeat steps (1) & (2)			

Remarks: Instrument Connection
*1: With a 470 µF/6.3 V capacitor to the TP2 (-) and J209/+B(+) "IC202".
*2: Mean Note 2 (See page 17)

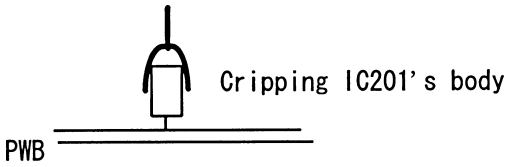
Note: AM TRACKING ERROR SPEC ≦ 6dB.

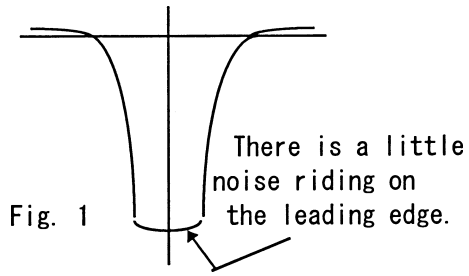
(4) Alignment for FM IF and FM Tracking

Step		Item	Required Instrument & Connection			Genescope or SG Freq.	Receiving Freq. (Set)	Adjust	Reading
			Instrument	Input	Output				
1		IF	Genescope	IC201 Note 3	TP1	10.7 MHz	High End (or 106.1 MHz)Freq.	T201	Max. Note 4
2	(1)	FM	FM signal	P1	TP1	90.2 MHz	90.2 MHz	L201	Max.
	(2)		Generator			106.1 MHz	106.1 MHz	CT201	
	(3)		400 Hz, 22.5 kHz Dev Note 6			Repeat steps (1) & (2)			

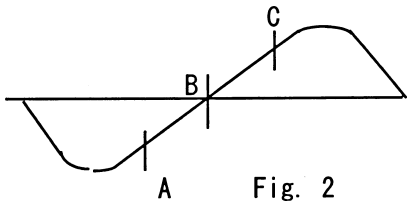
Note:

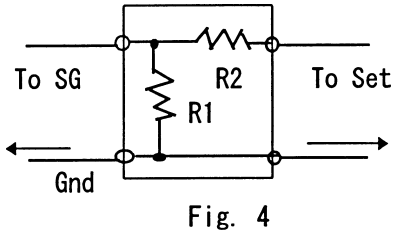
1. Feed in a week signal from the Genescope. Adjust T202 for max. gain and the waveform of Fig. 1.
2. Connect AM signal generator to loop antenna, bring near to ferrite antenna.
3. Input signal methode as follows.

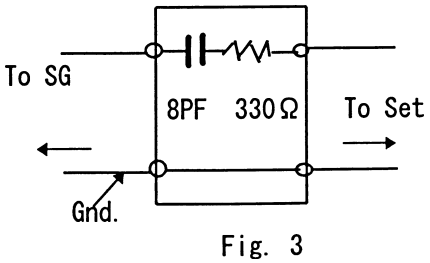




4. Feed in a week signal to IC201 (Note 3) from the genescope. Use the T201 core to from the S-curve shown in the Fig. 2.
   Adjust the symmetry of A and B about point C for linearity.
5. SW1, SW2 dummy antenna is shown in Fig. 3.
6. FM dummy antenna is shown in Fig. 4.







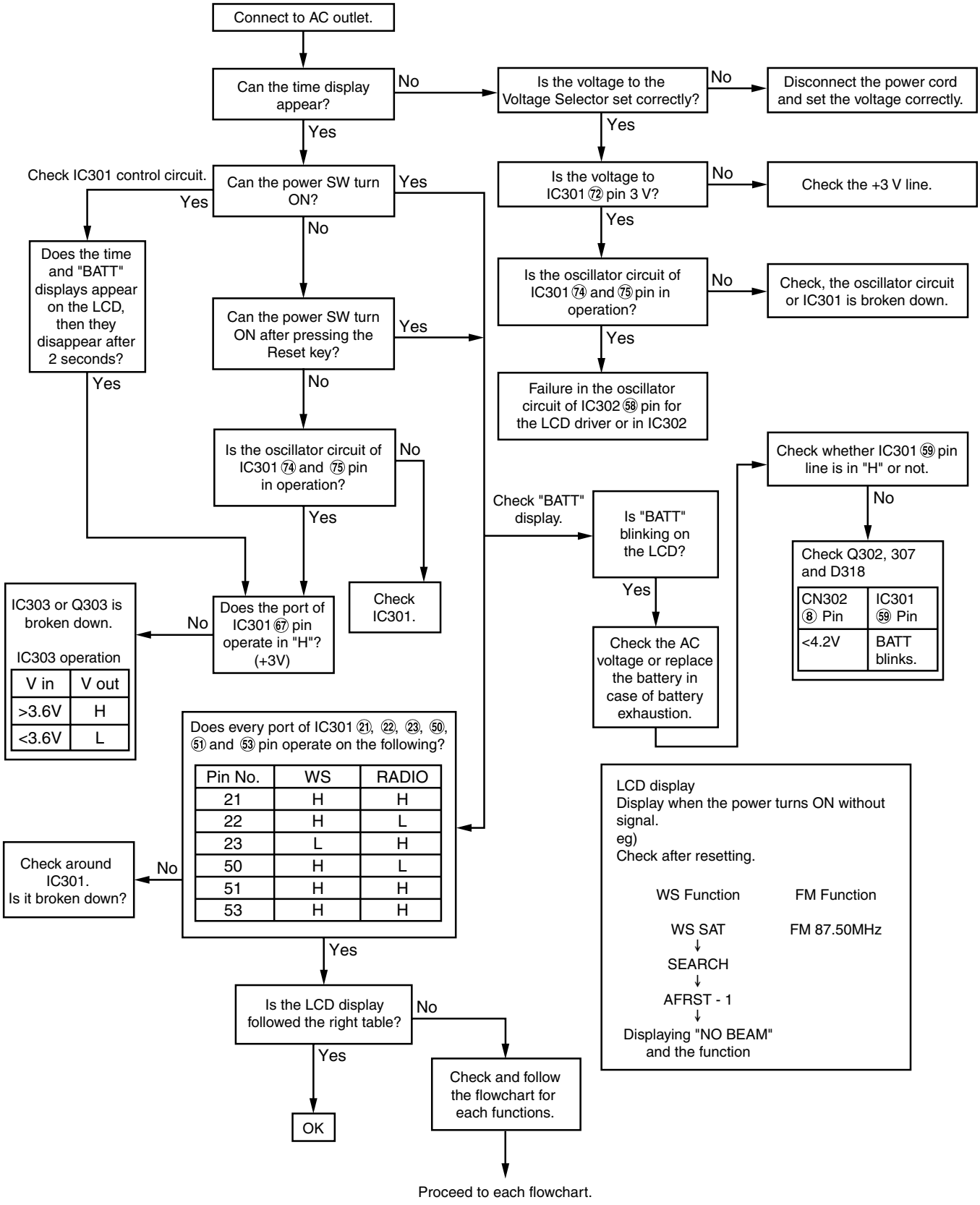
R1=Rg=SG's output impedance (75 Ω),
R2=75 - Rg/2

(5) Alignment for Clock Time Accuracy

Band	Adjustment	Procedure	Connection
FM	CT301	1) Tune FM to 108 MHz 2) Connect a Freq. Counter to J308 3) Adjust CT301 to reach the frequency 118.7 MHz ±1.5 kHz	To J308 ⟷ To Counter

TROUBLESHOOTING

1. System Check



2. WS section

(1) Determine whether WS circuit malfunctions or communications to control microcomputer malfunction.

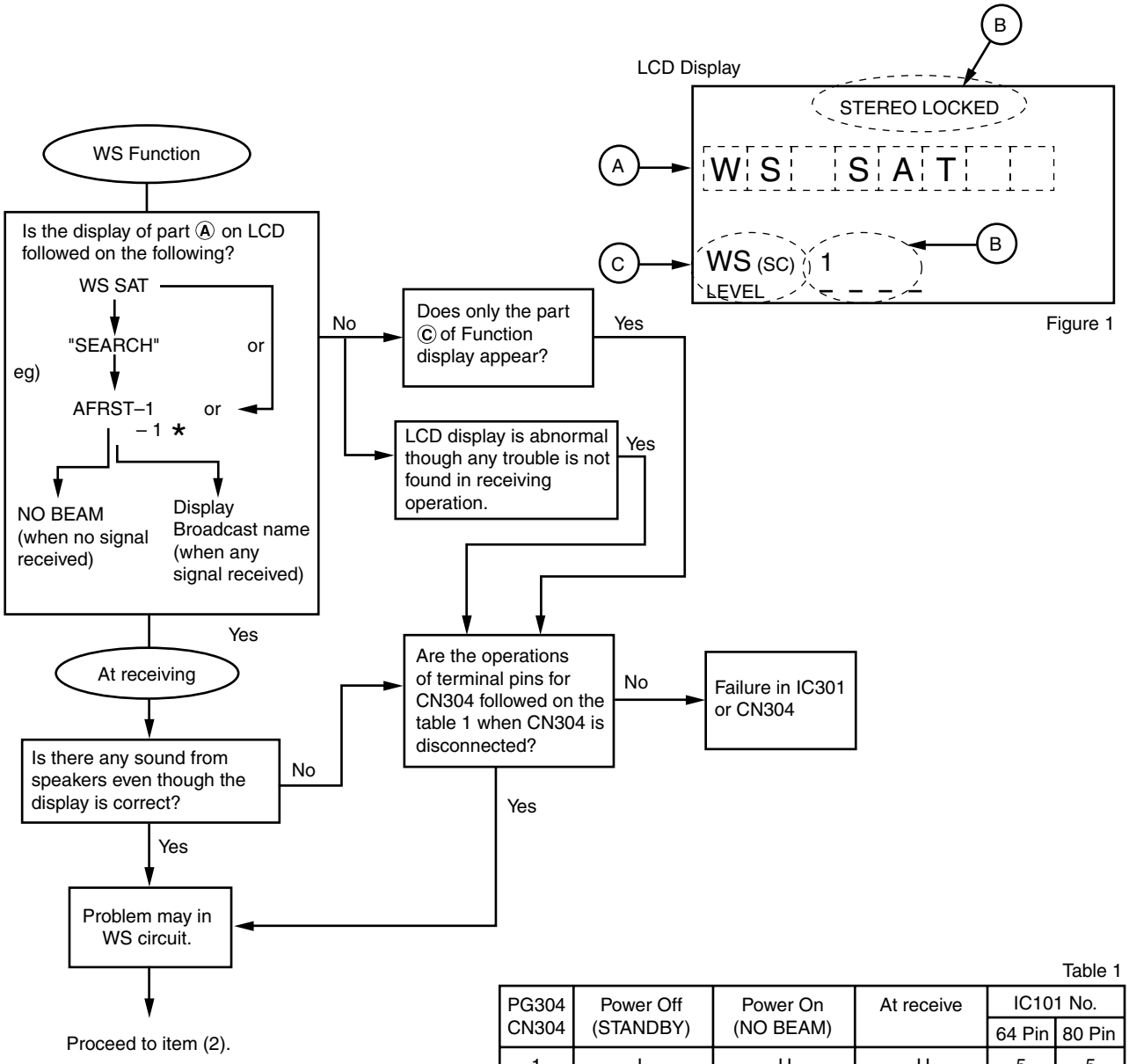


Figure 1

Table 1

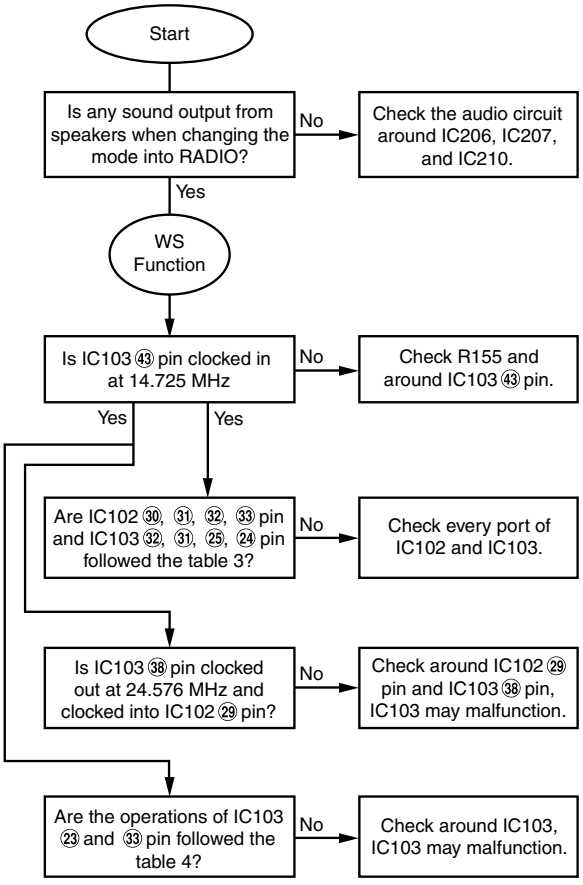
PG304 CN304	Power Off (STANDBY)	Power On (NO BEAM)	At receive	IC101 No.	
				64 Pin	80 Pin
1	L	H	H	5	5
2	(L) → H	H	H	4	4
3	Clock signal	←	←	3	3
5	Clock signal	←	←	2	2
6	L	L	Clock signal	1	1
7	H	H	H	7	7
8	L	L	L	57	71
9	L	Clock signal	←	59	74
10	L	Clock signal	←	58	72
11	L	L	L	60	75

(2) Checking and flowchart for WS circuit

Determine the display on LCD and the presence or absence of sound from speakers after turning the power ON.

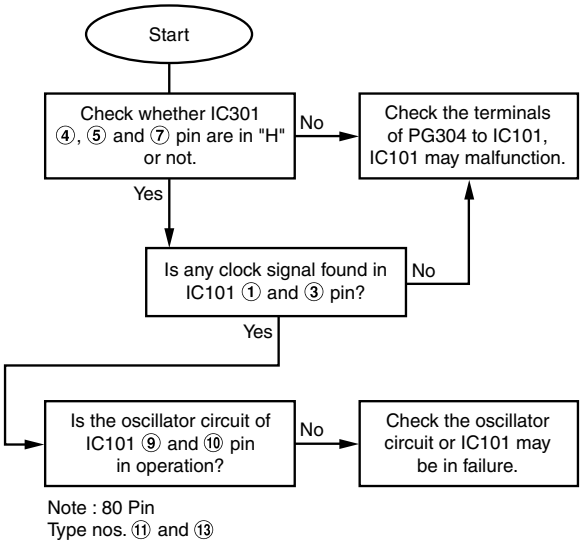
Note: The terminal number of IC101is assumed 64-pin type in the flowchart. For 80-pin type, refer to tables 1 to 4 and note.

① When no sound from speakers though any trouble is not found in receiving and display



② When no operation goes on

Only the part C of figure 1 or abnormal display will appear on LCD.



Note : 80 Pin
Type nos. ⑪ and ⑬

Table 2

IC101 No.		Power Off (STANDBY)	Power On (NO BEAM)	At receive	Connect to another IC	
64 Pin	80 Pin				IC102	IC103
28	36	L	H ⇄ L (reset)	H	—	7
29	37	L	H ⇄ L (reset)	H	—	41
30	38	L	H ⇄ L (reset)	H	27	40
32	40	L	H	H	—	39
33	41	L	L	Sync Pulse	21	—
41	52	L	L	Data signal	26	—
42	53	L	L	Clock signal	25	—
43	54	L	L	Data signal	24	—
46	58	L	H ⇄ L (reset)	H	28	—
47	59	L	H ⇄ L (reset)	H	20	2

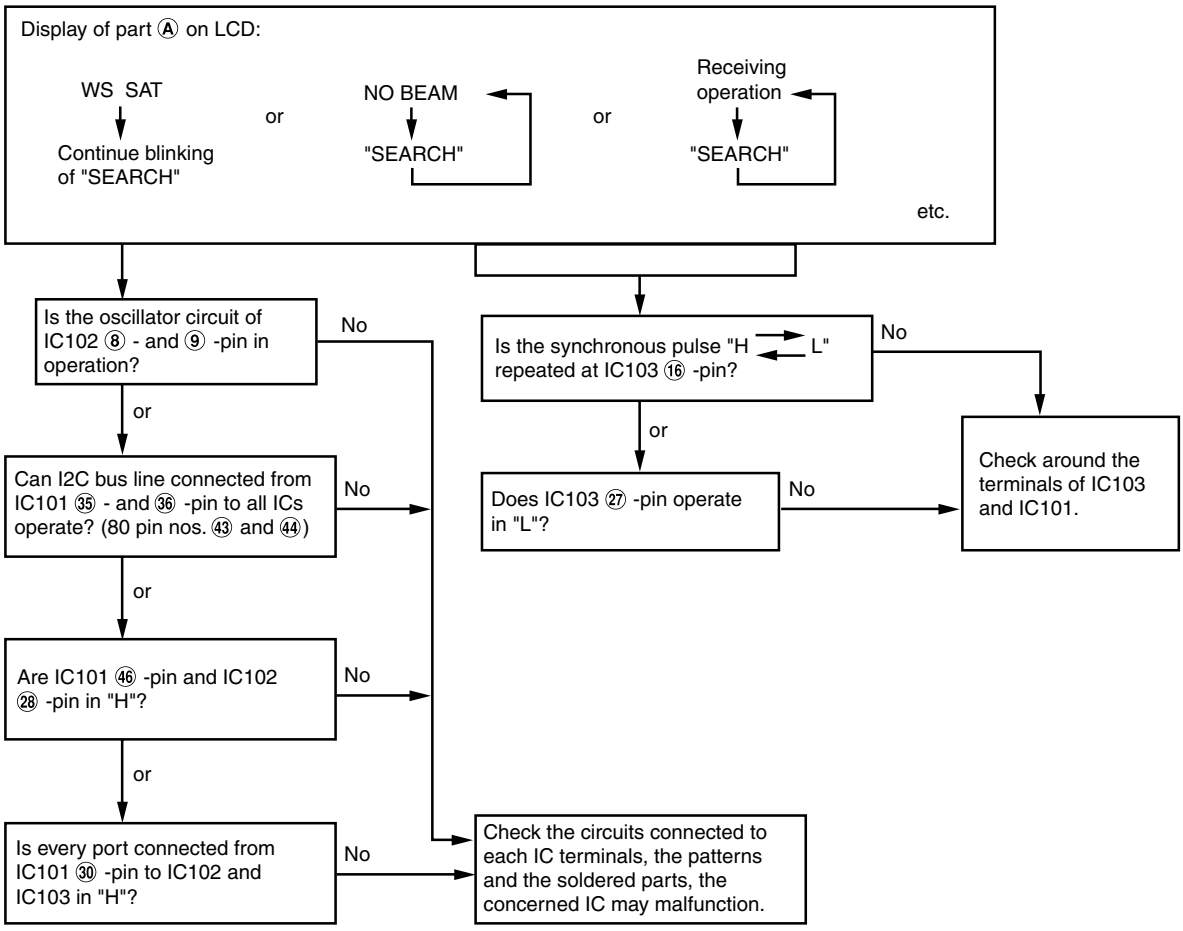
Table 3

IC102 No.	Power Off (STANDBY)	Power On (NO BEAM)	At receive	Connect to another IC
				IC103 No.
30	L	L	Clock signal	32
31	L	L	Data signal	30
32	L	24 kHz	8 kHz	25
33	L	L	Digital audio data	24

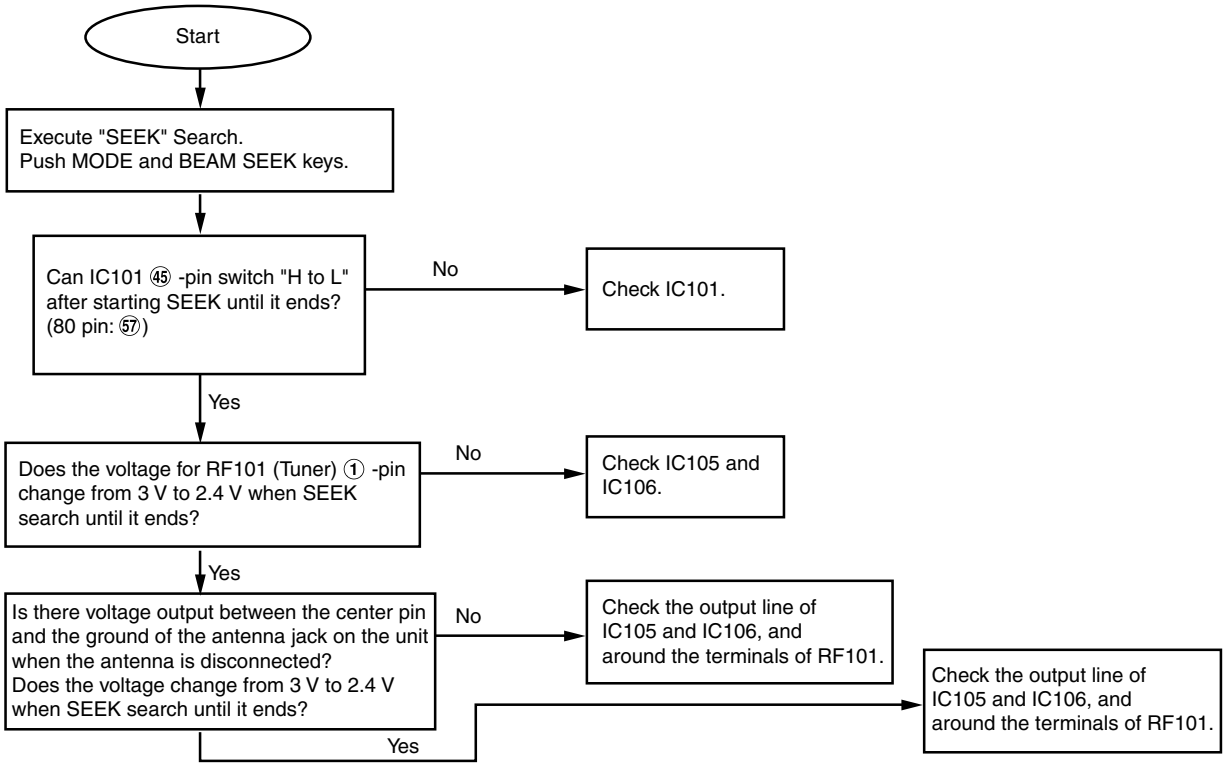
Table 4

IC102 No.	Power Off (STANDBY)	Power On (NO BEAM)	At receive	Connect to IC 101 No.	
				64 Pin	80 Pin
16	L	L	H ⇄ L (Sync puls)	27	35
22	L	L	H ⇄ L (Sync puls)	26	33
23	L	L	H	25	32
27	L	H	L	24	30
33	L	L	H	23	28

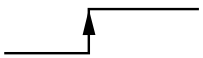
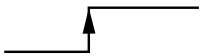
③ When the operation malfunctions after receiving operation starts



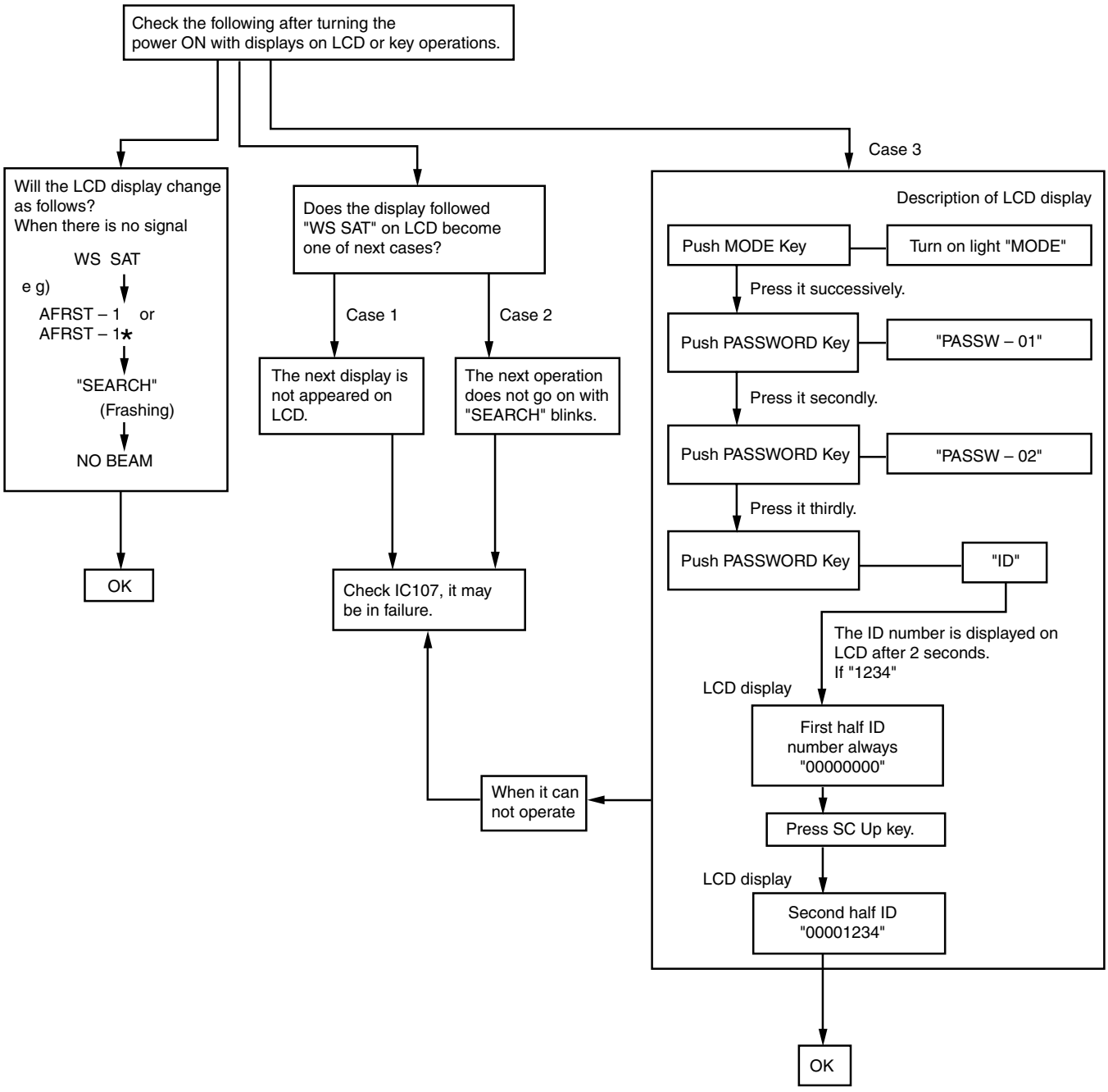
④ When the stations receivable with other units can not be received though the operation is proper



(3) Operations on WS functions after turning the power on

No	IC terminal no.	IC function / I/O	Data	Connect to	Check to confirm operation
1	IC101 47Pin (80pin No: 59)	WS RESET/Output		IC102 20pin IC103 2pin	Reset IC102 and IC103.
2	IC101 28Pin (80pin No: 36)	DCEN/Output		IC103 7pin	Turn IC103 on.
3	IC101 32Pin (80pin No: 40)	PUP IN/Input		IC103 39pin	Make sure IC103 is turned on.
4	IC101 46Pin (80pin No: 58)	PUP OUT/Output		IC102 28pin	Turn IC102 on.
5	IC102 12Pin (80pin No: 16)	Clock 14.725 MHz/Output	Clock waveform	IC103 43pin WS TUNER 8pin	IC103 generates 24.576 MHz from this clock (14.725MHz) for 38-pin out.
6	IC101 29Pin (80pin No: 37)	WRDY/Input		IC103 41pin	IC103 outputs a verification signal for the clock receiving.
7	IC101 35, 36Pin (80pin No: 43, 44)	I2 C BUS / I/O	I2 C BUS communication	IC102 22, 23pin	Set each IC to WS mode.
8	IC101 30Pin (80pin No: 38)	WSEN/Input		IC102 27pin IC103 40pin	IC101 inputs a verification signal that IC102 has been in WS mode.
9	IC101 33Pin (80pin No: 42)	SYNC/Input		IC102 21pin	IC102 responds that TSCC data has been received in WS mode.
10	IC101 35, 36Pin (80pin No: 43, 44)	I2 C BUS / I/O	I2 C BUS communication	IC102 22, 23pin	Microcomputer reads out the received TSCC data from IC102.

3. Check IC 24LC194 (IC107, E² PROM) of WS function



4. Radio Section

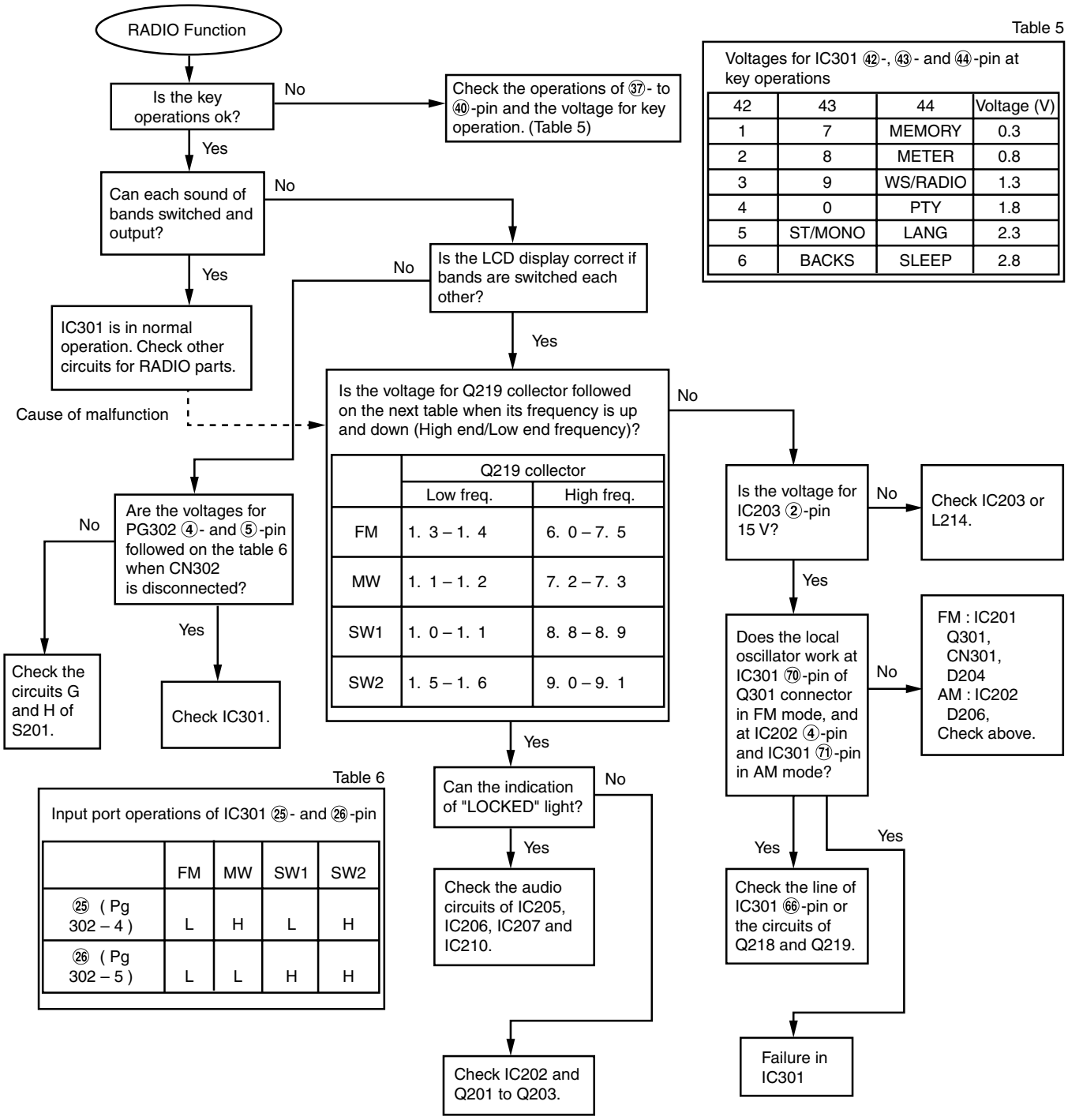


Table 5

Voltages for IC301 ㊷-, ㊸- and ㊹-pin at key operations

42	43	44	Voltage (V)
1	7	MEMORY	0.3
2	8	METER	0.8
3	9	WS/RADIO	1.3
4	0	PTY	1.8
5	ST/MONO	LANG	2.3
6	BACKS	SLEEP	2.8

	Q219 collector	
	Low freq.	High freq.
FM	1. 3 – 1. 4	6. 0 – 7. 5
MW	1. 1 – 1. 2	7. 2 – 7. 3
SW1	1. 0 – 1. 1	8. 8 – 8. 9
SW2	1. 5 – 1. 6	9. 0 – 9. 1

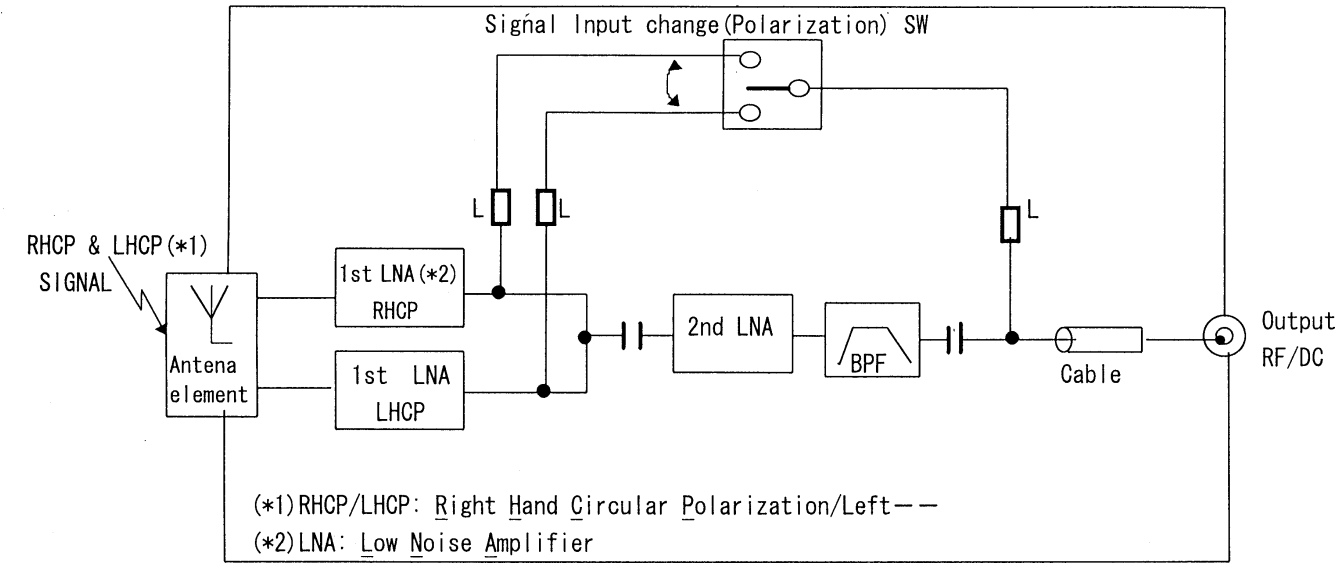
Table 6

Input port operations of IC301 ㉕- and ㉖-pin

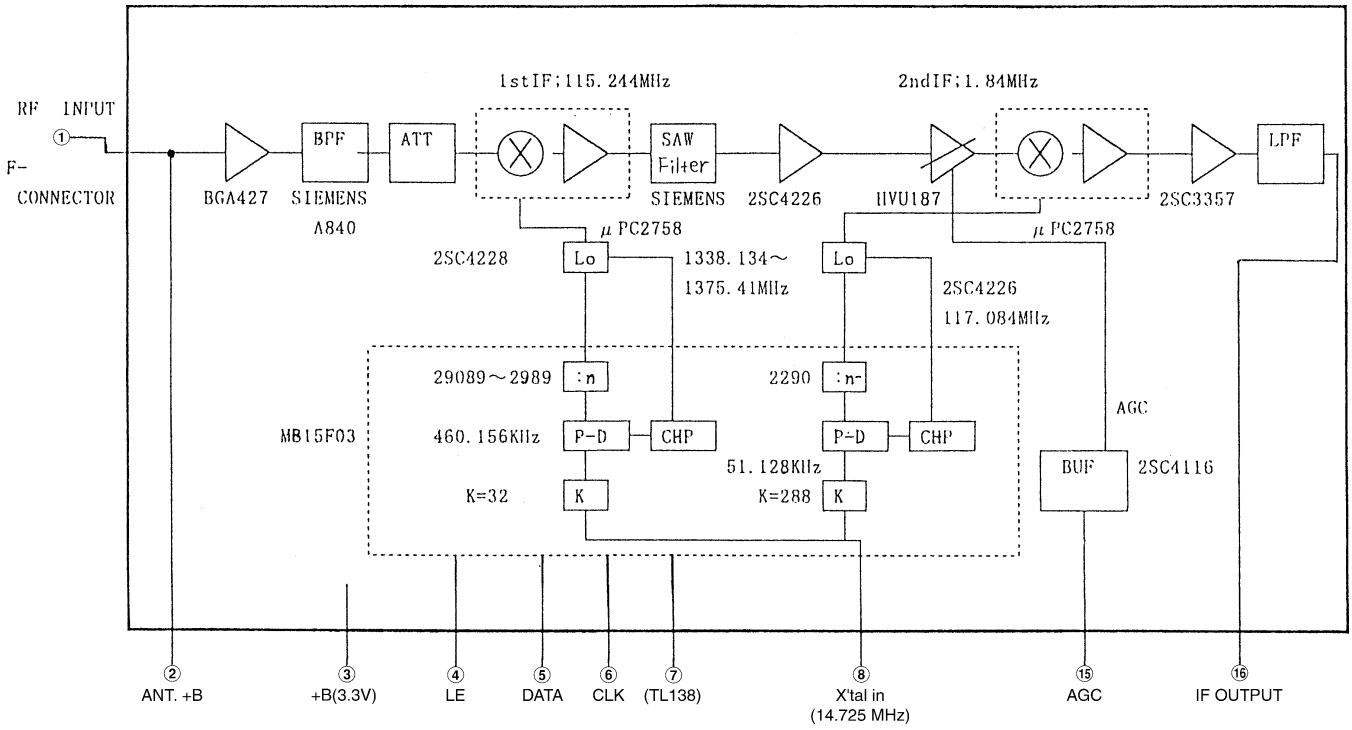
	FM	MW	SW1	SW2
㉕ (Pg 302 – 4)	L	H	L	H
㉖ (Pg 302 – 5)	L	L	H	H

BLOCK DIAGRAM OF ANTENNA AND TUNER UNIT

• Antenna Unit (RF001)

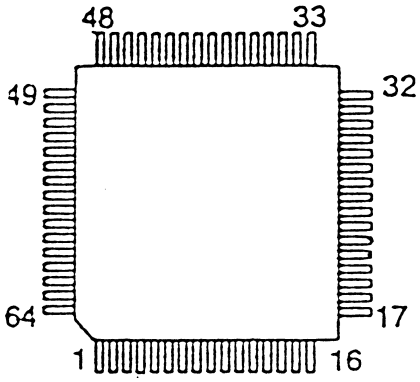


• Tuner Unit (RF101)



DATA OF MICROPROCESSOR

① In case 64 PIN type HD6472128FA20 or HD6432127RWV03FA

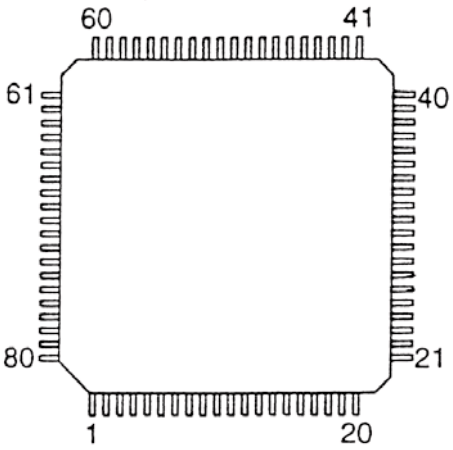


• Terminal Function

Pin No.	Symbol	I/O	Function
1	P50/TxD0	O	Signal data output
2	P51/RxD0	I	Signal data input
3	P52/SCK0	I/O	Clock input/output
4	$\overline{RES}$	I	When this pin is driven low, the chip is reset
5	NMI	I	WS POWER ON (Wake Up) signal input
6	VCC	–	+3.3 ∇ power supply
7	STBY	I	When this pin is driven high, hardware standby signal
8	VSS	–	Ground
9	XTAL	–	8.00 MHz Ceramic Oscillator connect
10	EXTAL	–	8.00 MHz Ceramic Oscillator connect
11	MD1	I	Mode pins setting to “H”
12	MD0	I	Mode pins setting to “H”
13	AVSS	–	Analog Ground
14	P70/AN0	I	Not used, setting to “L”
15	P71/AN1	I	WS POWER ON (Wake Up) signal input
16	P72/AN2	I	Not used, setting to “L”
17	P73/AN3	I	Not used, setting to “L”
18	P74/AN4	I	Not used, setting to “L”
19	P75/AN5	I	Not used, setting to “L”
20	P76/AN6	I	Not used, setting to “L”
21	P77/AN7	I	Not used, setting to “L”
22	AVCC	–	+3.3 ∇ analog power supply
23	P60	I	MPEG-FRAME-Sync signal input
24	P61	I	MPEG-CRC-ERROR signal input
25	P62	I	MPEG-BC-Sync signal input
26	P63	I	BC-FRAME-Sync signal input
27	P64	I	BC-FRAME-Toggle signal input
28	P65	O	DCEN signal output
29	P66	I	Ready signal input
30	P67	O	Enable signal input
31	VCC	–	+3.2 ∇ power supply

Pin No.	Symbol	I/O	Function
32	P27	I	Power up signal input
33	P26	I	Sync signal input
34	P25	I	Not used, setting to “L”
35	P24/SCL1	O	I^2C Serial bus line “clock”
36	P23/SDA1	O	I^2C Serial bus line “data”
37	P22	O	Not used, setting to “L”
38	P21	O	Not used, setting to “L”
39	P20	O	Not used, setting to “L”
40	VSS	–	Ground
41	P17	O	Not used pin
42	P16	O	Not used pin
43	P15	O	Not used pin
44	P14	–	Not used, setting to “L”
45	P13	O	L/R HCP change signal output LHCP = “L”
46	P12	O	Power up signal output
47	P11	O	Reset signal output
48	P10	I	Not used
49	P30	I	Fixing to “H”
50	P31	I	Not used, fixing to “L”
51	P32	I	Not used, fixing to “L”
52	P33	I	Not used, fixing to “L”
53	P34	I	Not used, fixing to “L”
54	P35	I	Not used, fixing to “L”
55	P36	I	Not used, fixing to “L”
56	P37	I	Not used, fixing to “L”
57	P40/IRQ2	I	STRB. signal input from Tuner µcon
58	P41/IRQ1	O	STRB. signal output to Tuner µcon
59	P42/IRQ0	I	ACK. signal input from Tuner µcon
60	P43	O	ACK. signal output to Tuner µcon
61	P44	I	Not used
62	P45	O	WS Audio mute signal output
63	P46	I	Not used
64	P47	O	Not used

② In case 80 PIN type HD6472128TF20

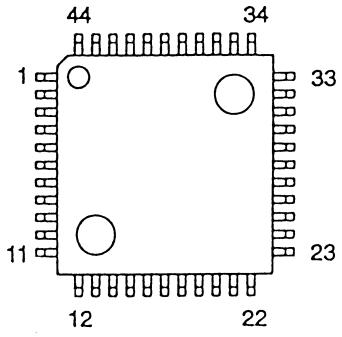


• Terminal Function

Pin No.	Symbol	I/O	Function
1	P50/TxD0	O	Signal data output
2	P51/RxD0	I	Signal data input
3	P52/SCK0	I/O	Clock input/output
4	$\overline{RES}$	I	When this pin is driven low, the chip is reset
5	NMI	I	WS POWER ON (Wake Up) signal input
6	VCC	–	+3.3 ∇ power supply
7	STBY	I	When this pin is driven high, hardware standby signal
8	VSS	–	Ground
9	VSS	–	Ground
10	VSS	–	Ground
11	XTAL	–	8.00 MHz Ceramic Oscillator connect
12	VSS	–	Ground
13	EXTAL	–	8.00 MHz Ceramic Oscillator connect
14	MD1	I	Mode pins setting to “H”
15	VSS	–	Ground
16	MD0	I	Mode pins setting to “H”
17	AVSS	–	Analog Ground
18	P70/AN0	I	Not used, setting to “L”
19	P71/AN1	I	WS POWER ON (Wake Up) signal input
20	P72/AN2	I	Not used, setting to “L”
21	P73/AN3	I	Not used, setting to “L”
22	P74/AN4	I	Not used, setting to “L”
23	P75/AN5	I	Not used, setting to “L”
24	VSS	–	Ground
25	P76/AN6	I	Not used, setting to “L”
26	P77/AN7	I	Not used, setting to “L”
27	AVCC	–	+3.3 ∇ analog power supply
28	P60	I	MPEG-FRAME-Sync signal input
29	VSS	–	Ground
30	P61	I	MPEG-CRC-ERROR signal input
31	VSS	–	Ground
32	P62	I	MPEG-BC-Sync signal input
33	P63	I	BC-FRAME-Sync signal input
34	VSS	–	Ground
35	P64	I	BC-FRAME-Toggle signal input
36	P65	O	DCEN signal output
37	P66	I	Ready signal input
38	P67	O	Enable signal input
39	VCC	–	+3.2 ∇ power supply

Pin No.	Symbol	I/O	Function
40	P27	I	Power up signal input
41	P26	I	Sync signal input
42	P25	I	Not used, setting to “L”
43	P24/SCL1	O	I^2C Serial bus line “clock”
44	P23/SDA1	O	I^2C Serial bus line “data”
45	VSS	–	Ground
46	P22	O	Not used, setting to “L”
47	P21	O	Not used, setting to “L”
48	P20	O	Not used, setting to “L”
49	VSS	–	Ground
50	VSS	–	Ground
51	VSS	–	Ground
52	P17	O	Not used pin
53	P16	O	Not used pin
54	P15	O	Not used pin
55	VSS	–	Ground
56	P14	–	Not used, setting to “L”
57	P13	O	L/R HCP change signal output LHCP = “L”
58	P12	O	Power up signal output
59	P11	O	Reset signal output
60	P10	I	Not used
61	P30	I	Fixing to “H”
62	P31	I	Not used, fixing to “L”
63	P32	I	Not used, fixing to “L”
64	P33	I	Not used, fixing to “L”
65	P34	I	Not used, fixing to “L”
66	VSS	–	Ground
67	P35	I	Not used, fixing to “L”
68	P36	I	Not used, fixing to “L”
69	P37	I	Not used, fixing to “L”
70	VSS	–	Ground
71	P40/IRQ2	I	STRB. signal input from Tuner µcon
72	P41/IRQ1	O	STRB. signal output to Tuner µcon
73	VSS	–	Ground
74	P42/IRQ0	I	ACK. signal input from Tuner µcon
75	P43	O	ACK. signal output to Tuner µcon
76	VSS	–	Ground
77	P44	I	Not used
78	P45	O	WS Audio mute signal output
79	P46	I	Not used
80	P47	O	Not used

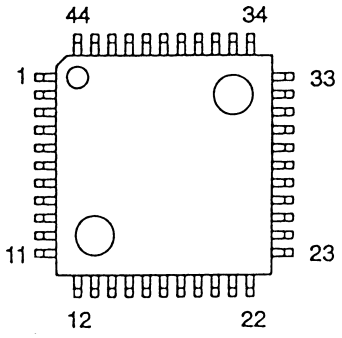
DRD3515A-QG-E3 (IC102)



• DRD3515A Terminal Function

Pin No. QFP	Pin Name	Type	Description
1	AGNDC	BID	Analog reference ground
2	AVSS1	SUPPLY	Analog ground for audio stages
3	AVSS0	SUPPLY	Analog ground for audio output amplifiers
4	OUT1	OUT	Not used
5	OUT2	OUT	Not used
6	AVDD0	SUPPLY	Power supply for audio output amplifiers
7	AVDD1	SUPPLY	Power supply for audio stages
8	XTI	IN	14.725 MHz quartz oscillator pin 1
9	XTO	OUT	14.725 MHz quartz oscillator pin 2
10	AVDD2	SUPPLY	VDD for IF input
11	AVSS2	SUPPLY	VSS for IF input
12	RCLK	OUT	Output reference frequency
13	SGND	IN	Signal GND for IF input
14	IFIN	IN	Differential IF input
15	IFINQ	IN	Differential IF input inverted
16	VREFI	BID	Reference for IF input
17	VSS	SUPPLY	Digital VSS
18	VDD	SUPPLY	Digital VDD
19	TEQ	IN	“H” digital VDD
20	PORQ	IN	Power On Reset, active low
21	SYNC	OUT	TSCC mode : TSCC data ready BC mode : Decryption data from new SCH available
22	SDA	BID	I^2C Data Line
23	SCL	BID	I^2C Clock Line
24	SCC	OUT	Service Component Clock
25	SCD	OUT	Service Component Data
26	SBCW	OUT	Service Component Wordstrobe
27	WSEN	OUT	WorldSpace enable output
28	PUP	IN	Power up
29	OCLK	IN	24.576 MHz input oversampling clock
30	BCC	OUT	Broadcast Channel clock
31	BCD	OUT	Broadcast Channel data
32	DAI	IN	Digital Audio Frame Identification
33	DAD	IN	Digital Audio Data
34	AUX2L	IN	AUX2 left input for external analog signals (not used)
35	AUX2R	IN	AUX2 right input for external analog signals (not used)
36	AUX1L	IN	AUX1 left input for external analog signals (not used)
37	AUX1R	IN	AUX1 right input for external analog signals (not used)
38	FOUTL	OUT	Output to left external filter
39	FOPL	BID	Filter op-amp inverting input, left
40	FINL	OUT	Filter op-amp output (line out)
41	FOUTR	OUT	Output to right filter op-amp
42	FOPR	BID	Right filter op-amp inverting input
43	FINR	OUT	Filter op-amp output (line out)
44	VREF	IN	Analog reference voltage

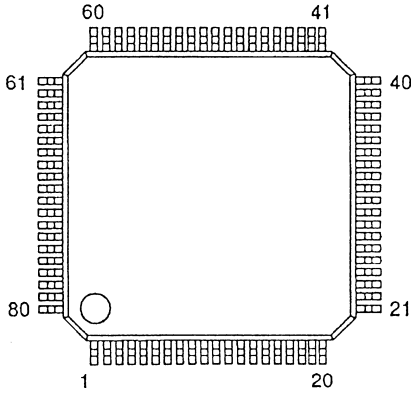
MAS3506D-QG-E9 (IC103)



• DRD3515A Terminal Function

Pin No. QFP	Pin Name	Type	Description
1	TE	I	Test Enable / Not used / Connected to Ground
2	PORQ	I	Power ON RESET, Active Low
3	I2CC	I O	I^2C Clock Line
4	I2CD	I O	I^2C Data Line
5	VDD	SUPPLY	Power Supply for Digital Parts (+3.2 ∇)
6	VSS	SUPPLY	Ground Supply for Digital Parts
7	DCEN	I	Voltage Supervision
8	EOD	O	Not used
9	RTR	O	Not used
10	RTW	O	Not used
11	DCSG	SUPPLY	Ground
12	DCSO	O	Open Drain “L” / Not used
13	VSENS	I	DC Converter Voltage Sense
14	PR	I	PIO DMA Request or Read/Write
15	PCS	I	PIO Chip Select, Active Low
16	PI19	O	BC-Frame-Toggle
17	PI18	I	BCINENABLEQ
18	PI17	I	PIO Data [17], reserved
19	SIC*	I	PIO Data [16] (SIC*)
20	SII*	I	PIO Data [15] (SII*)
21	SID*	I	PIO Data [14] (SID*)
22	PI13	O	MPEG-FRAME-SYNC
23	PI12	O	BC-SYNC
24	SOD	O	Serial Output Data
25	SOI	O	Serial Output Frame Identification
26	SOC	O	Serial Output Clock
27	PI8	O	MPEG-CRC-Error
28	XVDD	SUPPLY	Positive Supply of Output Buffers
29	XVSS	SUPPLY	Ground of Output Buffers
30	SID	I	Serial Input Data
31	SII	I	Serial Input Frame Identification
32	SIC	I	Serial Input Clock
33	PI4	O	MPEG-FRAME-SYNC
34	PI3	I	AUD-SW, information from headphone jack
35	PI2	I	Reserved
36	PI1	I	Reserved
37	PI0	I	Reserved
38	CLKO	O	Clock Output (nominal 24.576 MHz)
39	PUP	O	Power Up, i.e. Status of Voltage Supervision
40	WSEN	I	WS Enable : Enable Layer 3 Decoding
41	WRDY	O	WSEN = 0 : Valid clock input at CLKI WSEN = 1 : Clock synthesizer locked to Broadcast Channel data stream
42	AVDD	SUPPLY	Supply for Analog Circuits
43	CLKI	I	Clock Input
44	AVSS	SUPPLY	Ground Supply for Analog Circuits

TC9327F-200 or -800 (IC301)



• Terminal Function

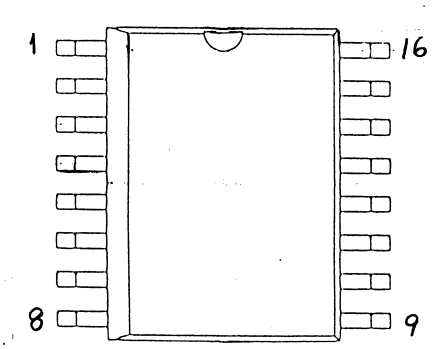
Pin No.	Terminal	I/O	Function
1	COM 1	OUT	Not used
2	COM 2	OUT	Not used
3	COM 3	OUT	Not used
4	COM 4	OUT	Not used
5	S 1	OUT	Not used
6	S 2	OUT	Not used
7	S 3	OUT	Not used
8	S 4	OUT	Not used
9	S 5	OUT	Not used
10	S 6	OUT	Not used
11	S 7	OUT	Not used
12	S 8	OUT	Not used
13	S 9	OUT	Not used
14	S 10	OUT	Not used
15	S 11	OUT	Not used
16	S 12	OUT	Not used
17	S 13	OUT	Not used
18	S 14	OUT	Not used
19	S 15	OUT	Not used
20	S 16	OUT	Not used
21	AUDIO	OUT	Function Output Port output will be set as the following table according to the currently received function. OFF / WS / RADIO AUDIO: L / H / H WS: L / H / L RADIO: L / L / H
22	WS	OUT	
23	RADIO	OUT	
24	N.C.	OUT	Not used
25	BAND 0	IN	Band Input Set port input as the following table in accordance with the currently receiving band. FM / MW / SW1 / SW2 BAND 0: L / H / L / H BAND 1: L / L / H / H BAND 2: L / L / L / L
26	BAND 1	IN	
27	BAND 2	IN	

Pin No.	Terminal	I/O	Function
28	N.C.	OUT	Not used
29	T7 (P9-0)	OUT	KEY TIMING O/P TERMINAL
30	T6 (P9-1)	OUT	
31	T5 (P9-2)	OUT	
32	T4 (P9-3)	OUT	Not used
33	N.C.	OUT	Not used
34	K0 (KEY IN)	IN	KEY I/P TERMINAL
35	K1 (KEY IN)	IN	
36	K2 (KEY IN)	IN	
37	K3 (KEY IN)	IN	
38	T0 (P1-0)	OUT	KEY TIMING O/P TERMINAL
39	T1 (P1-1)	OUT	
40	T2 (P1-2)	OUT	
41	T3 (P1-3)	OUT	Not used
42	AD IN 1	IN	KEY I/P TERMINAL
43	AD IN 2	IN	
44	AD IN 3	IN	
45	DCREF	IN	Not used
46	SDR (SI)	IN	SERIAL DATA I/P TERMINAL
47	SDATA (SO)	OUT	SERIAL DATA O/P TERMINAL
48	SCK	OUT	SERIAL LOCK O/P TERMINAL
49	CE (LCD)	OUT	LCD CHIP ENABLE O/P TERMINAL
50	WS ON (POWER)	OUT	WS ON O/P TERMINAL
51	WS RESET	OUT	WS RESET O/P TERMINAL
52	N.C.	OUT	Not used
53	WS STBY	OUT	WS STBY O/P TERMINAL
54	DTS STB	OUT	DTS CHIP ENABLE O/P TERMINAL
55	DTS ACK	OUT	DTS ACKNOWLEDGE O/P TERMINAL
56	M STB	IN	MICON CHIP ENABLE I/P TERMINAL
57	M ACK	IN	MICON ACKNOWLEDGE I/P TERMINAL
58	ST IN	IN	STEREO I/P
59	$\overline{\text{BATTERY IN}}$	IN	BATTERY REMAINING I/P
60	ST/MONO	OUT	STEREO/MONO O/P
61	SD IN	IN	ST DETECTION I/P L : DETECTED
62	MUTE	OUT	MUTING O/P H : MUTE L : OFF
63	TEST	IN	Not used
64	IF IN	IN	IF SIGNAL I/P TERMINAL
65	PLL OUT	OUT	PLL O/P TERMINAL
66	PLL OUT	OUT	PLL O/P TERMINAL
67	HOLD IN	IN	BACKUP MODE CANCELLING
68	LIGHT	OUT	LIGHT O/P (Not used)
69	GND	—	GND TERMINAL
70	FM IN	IN	FM OSC input
71	AM IN	IN	AM OSC input
72	VDD	—	+3.0 ∇ power supply
73	RESET	IN	SYS RESET SIGNAL I/P TERMINAL Connect to VDD
74	XOUT	—	75 kHz X'tal oscillator connect
75	XIN	—	75 kHz X'tal oscillator connect
76	VXT	—	POWER FILTER TERMINAL
77	VLCD	—	Connect to VDD
78	C1	—	Not used
79	C2	—	Not used
80	VEE	—	Not used

SEMICONDUCTORS

• IC's

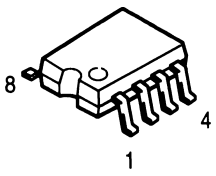
PCF8574AT (IC104)



PCF8574AT Terminal Function

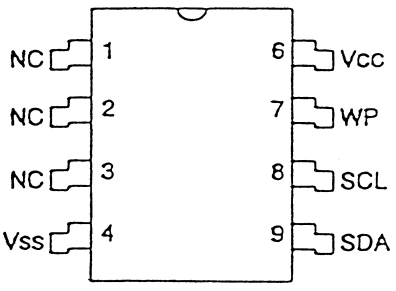
Pin No.	Symbol	Description
1	(AO)	Address input 0 not used fixed "H"
2	(A1)	Address input 1 not used fixed "H"
3	(A2)	Address input 2 not used fixed "H"
4	(P0) CLK	Quasi-bidirectional I/O 0
5	(P1) DATA	Quasi-bidirectional I/O 1
6	(P2) EN	Quasi-bidirectional I/O 2
7	P3	Quasi-bidirectional I/O 3
8	VSS	Supply ground
9	(P4)	Quasi-bidirectional I/O 4 not used
10	(P5)	Quasi-bidirectional I/O 5 not used
11	(P6)	Quasi-bidirectional I/O 6 not used
12	(P7)	Quasi-bidirectional I/O 7 not used
13	$\overline{(INT)}$	Interrupt output (active low) not used
14	SCL	Serial clock line
15	SDA	Serial data line
16	VDD	Supply voltage

24LC194 (IC107)

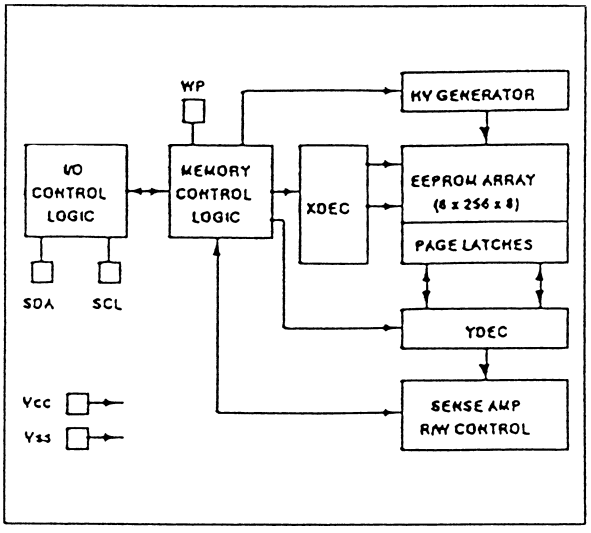


Pin Function

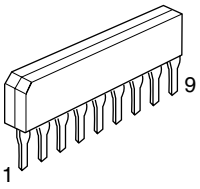
Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+3.2 ∇ Power Supply
NC	No Internal Connection Fixed "L"

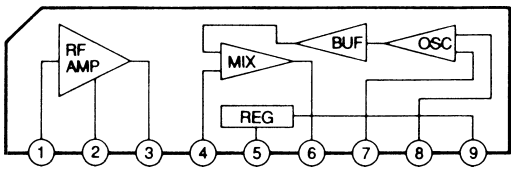


Block Diagram

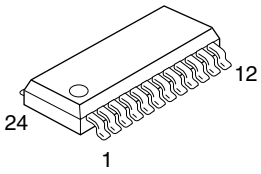


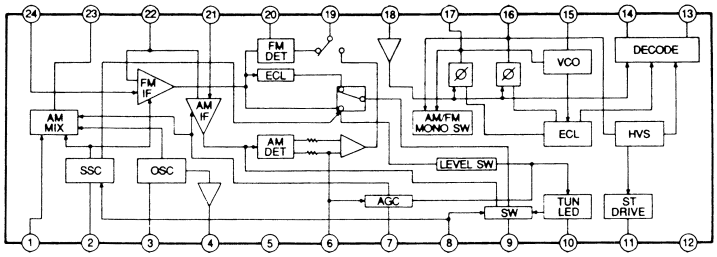
TA7358AP (IC201)



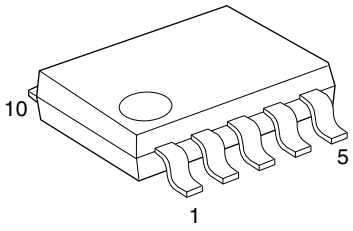


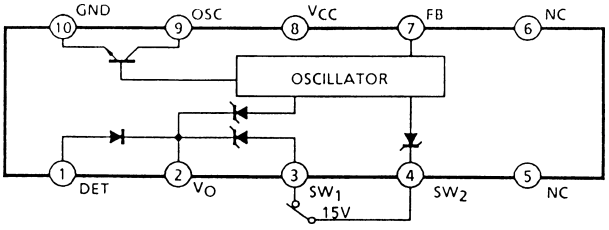
TA8132AF (IC202)



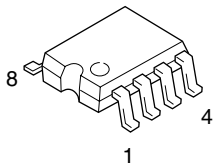


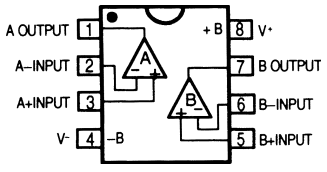
TA8126F (IC203)



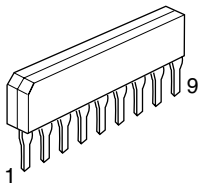


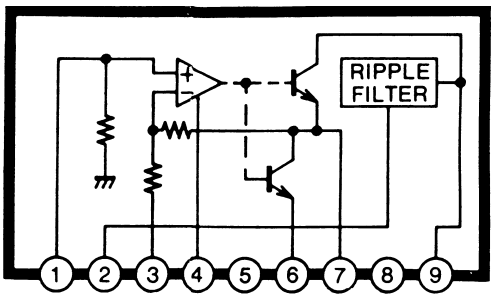
BA4510F (IC205, 210)



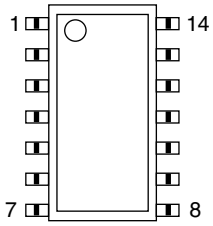


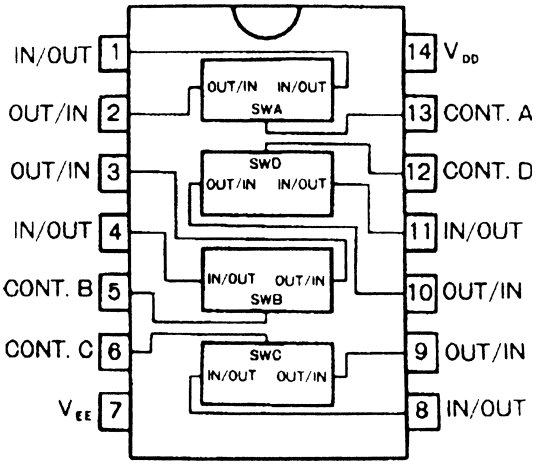
TA7368P (IC206, 207)



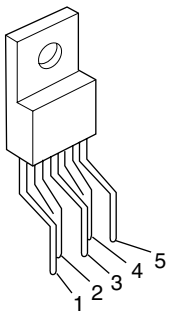


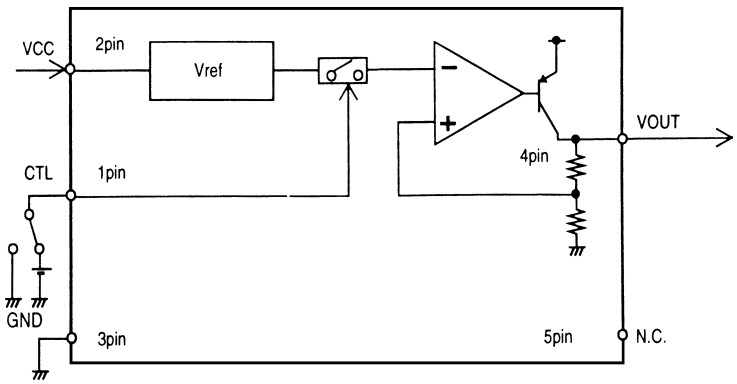
BU4066BCF (IC204)



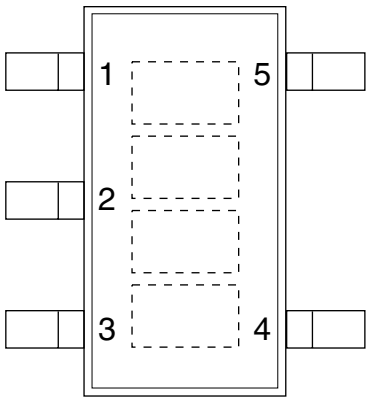


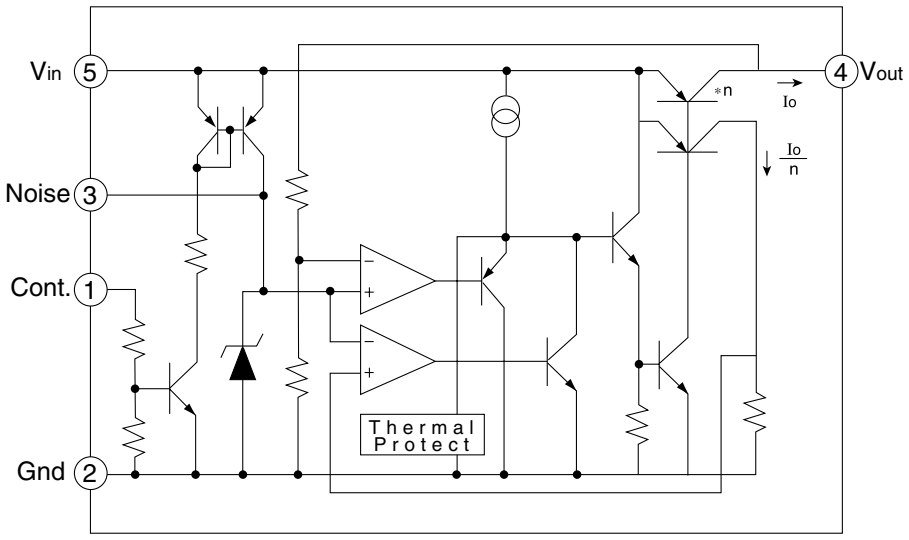
BA033ST-V5 (IC209)



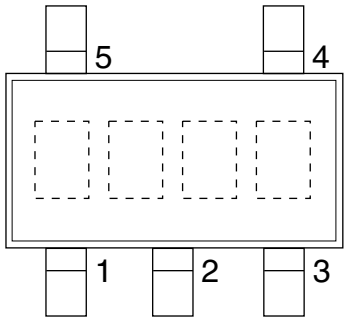


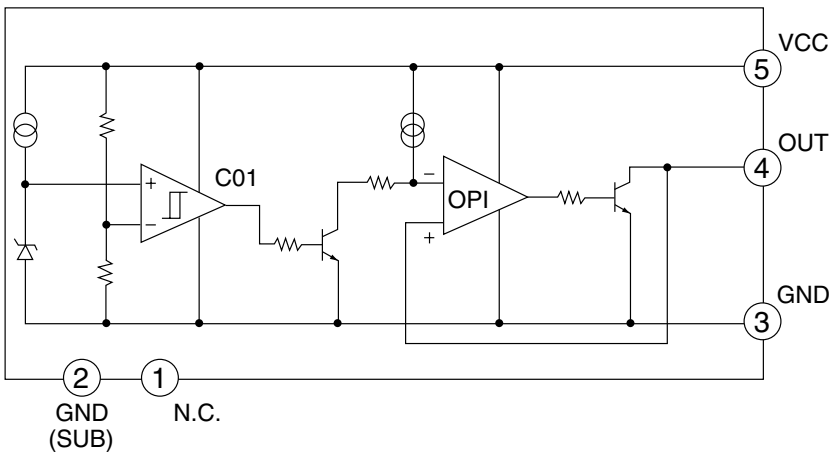
MM1385D (IC208)
MM1385H (IC105)
MM1385P (IC106)



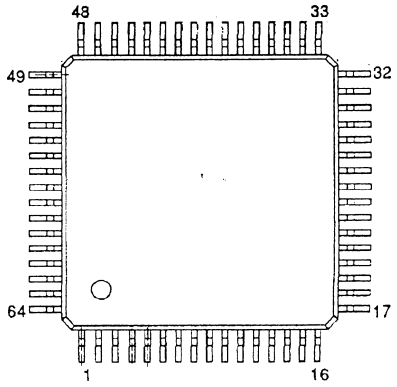


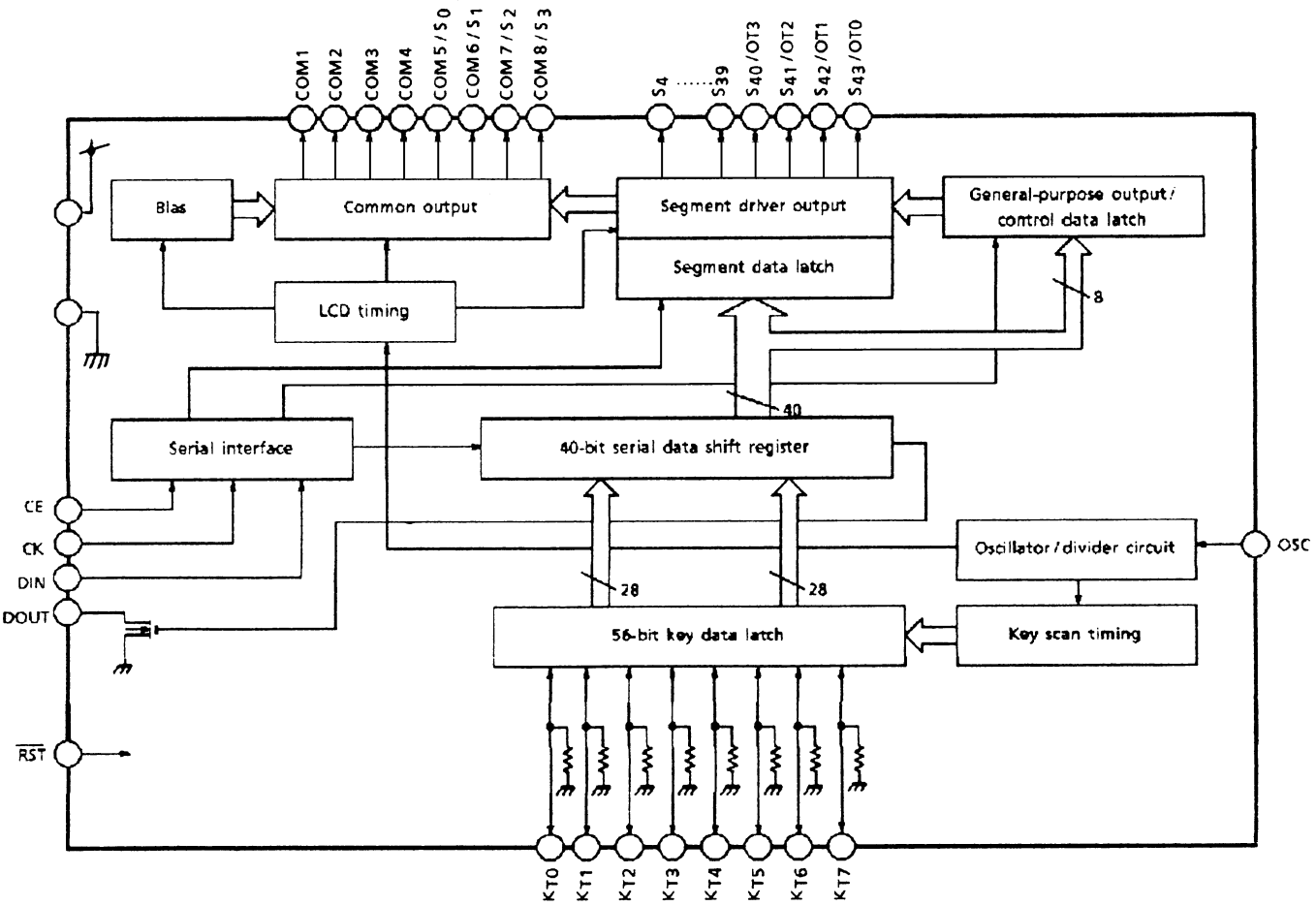
PST9136N (IC303)





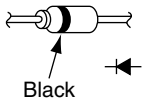
TC9298F (IC302)



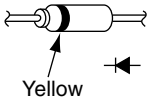


• DIODES (including LED)

1N4531



1SS133



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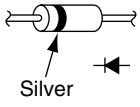
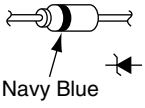
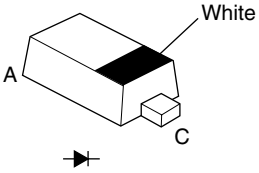


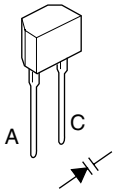
MTZ-J3.6B



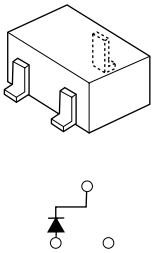
1SS355
FM4002



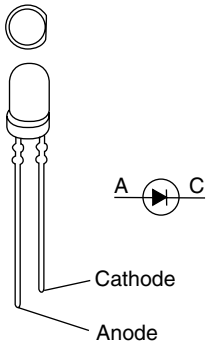
1SV149
1SV101



RB461F

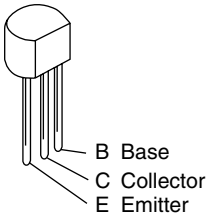


SLR56VC3F (RED)

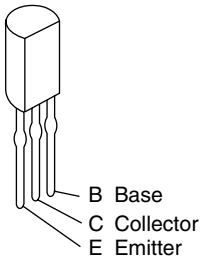


• TRANSISTORS

HIT9016G



2SA1020 (Y)



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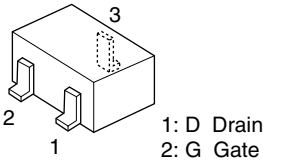
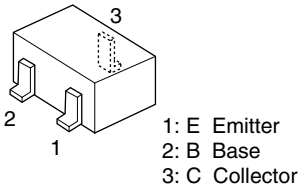
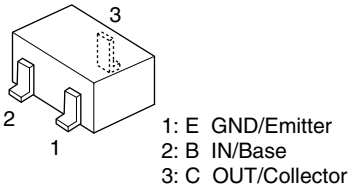


2SC2412K
2SA1037AK (Q/R)
2SD1757K (Q/R)
2SD1048



DTC124EK
DTA144GKA



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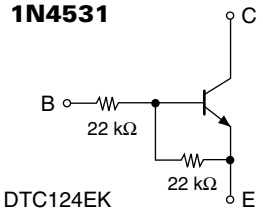

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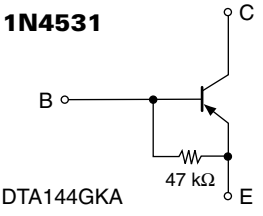
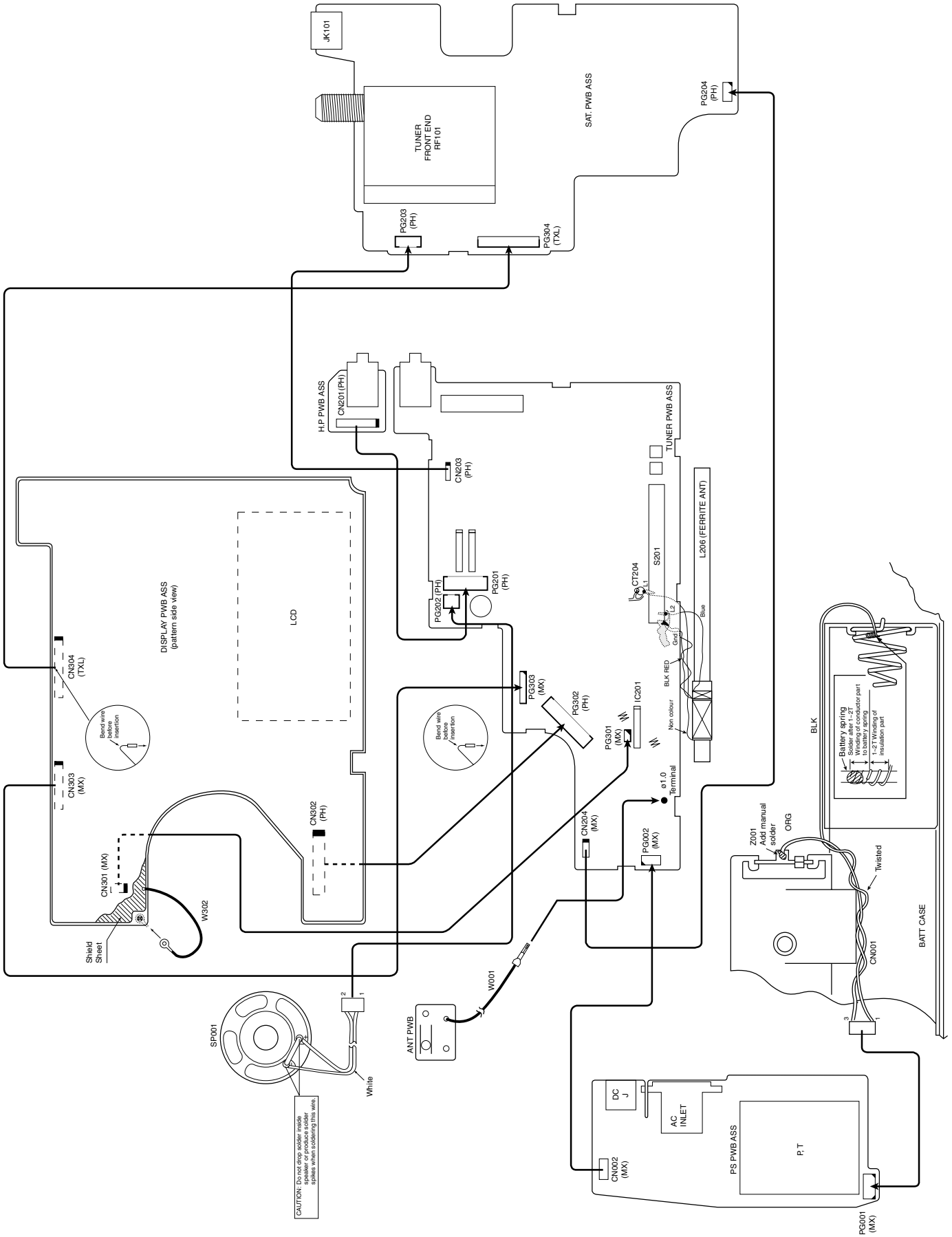
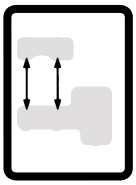


WIRING DIAGRAM

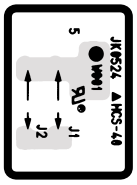


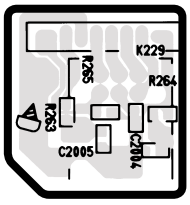
PRINTED WIRING BOARD

Soldering Side *Component Side*

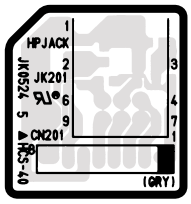


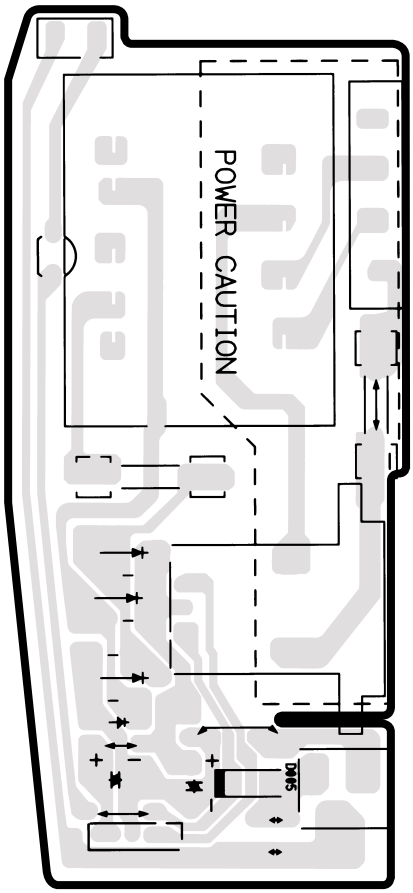
ANTENNA PWB



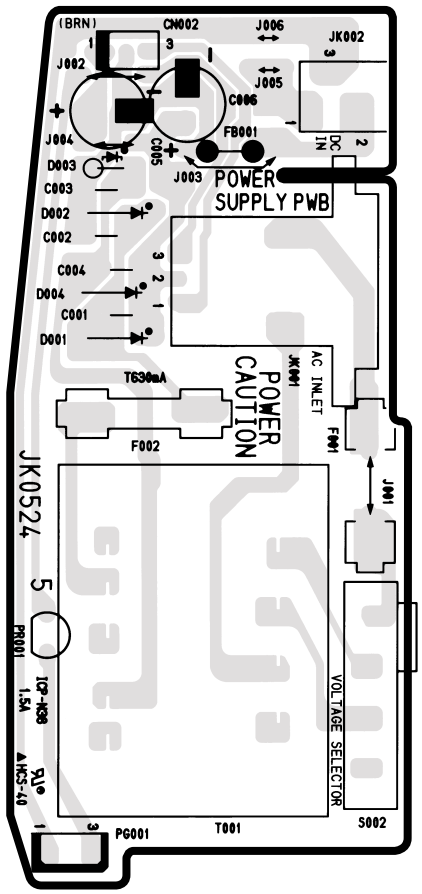


HEADPHONE PWB

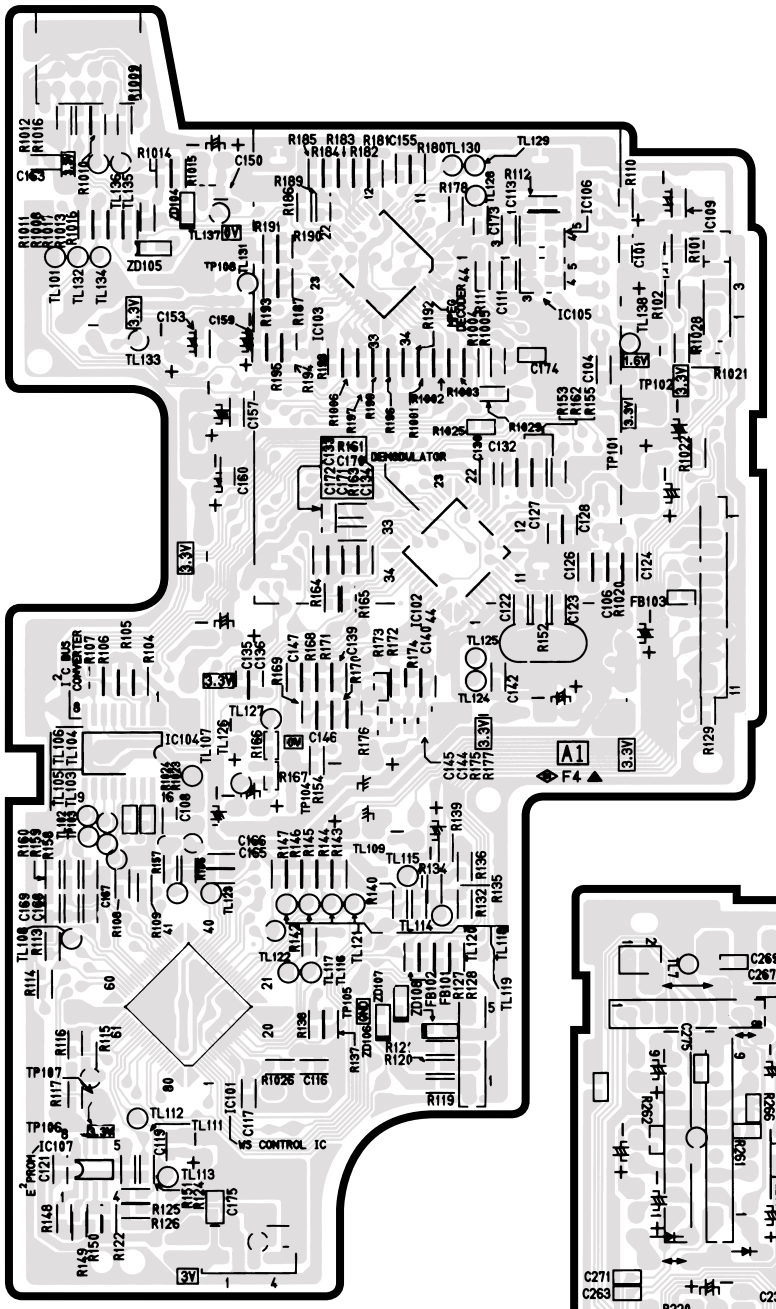




POWER SUPPLY PWB

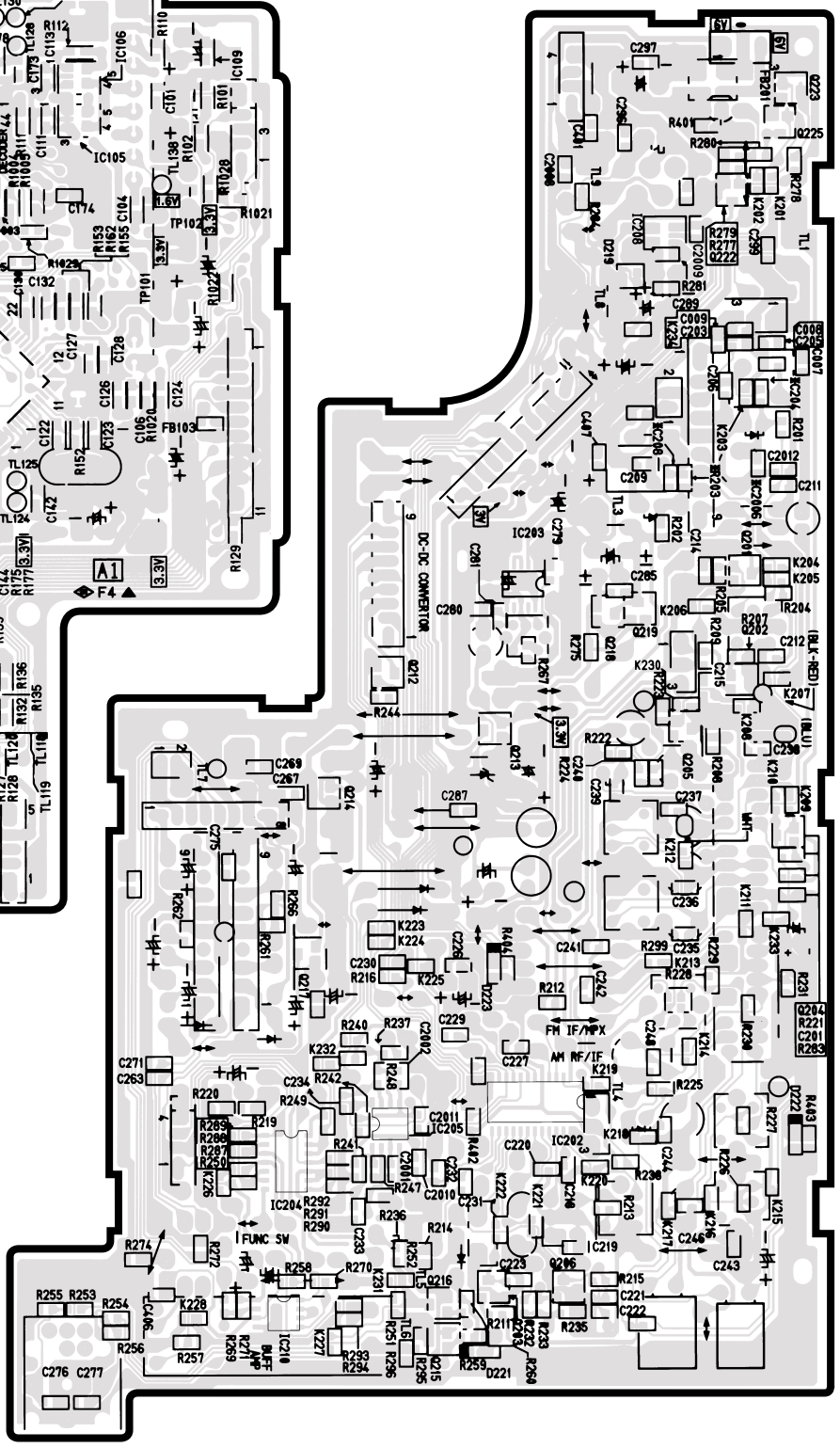


Soldering Side



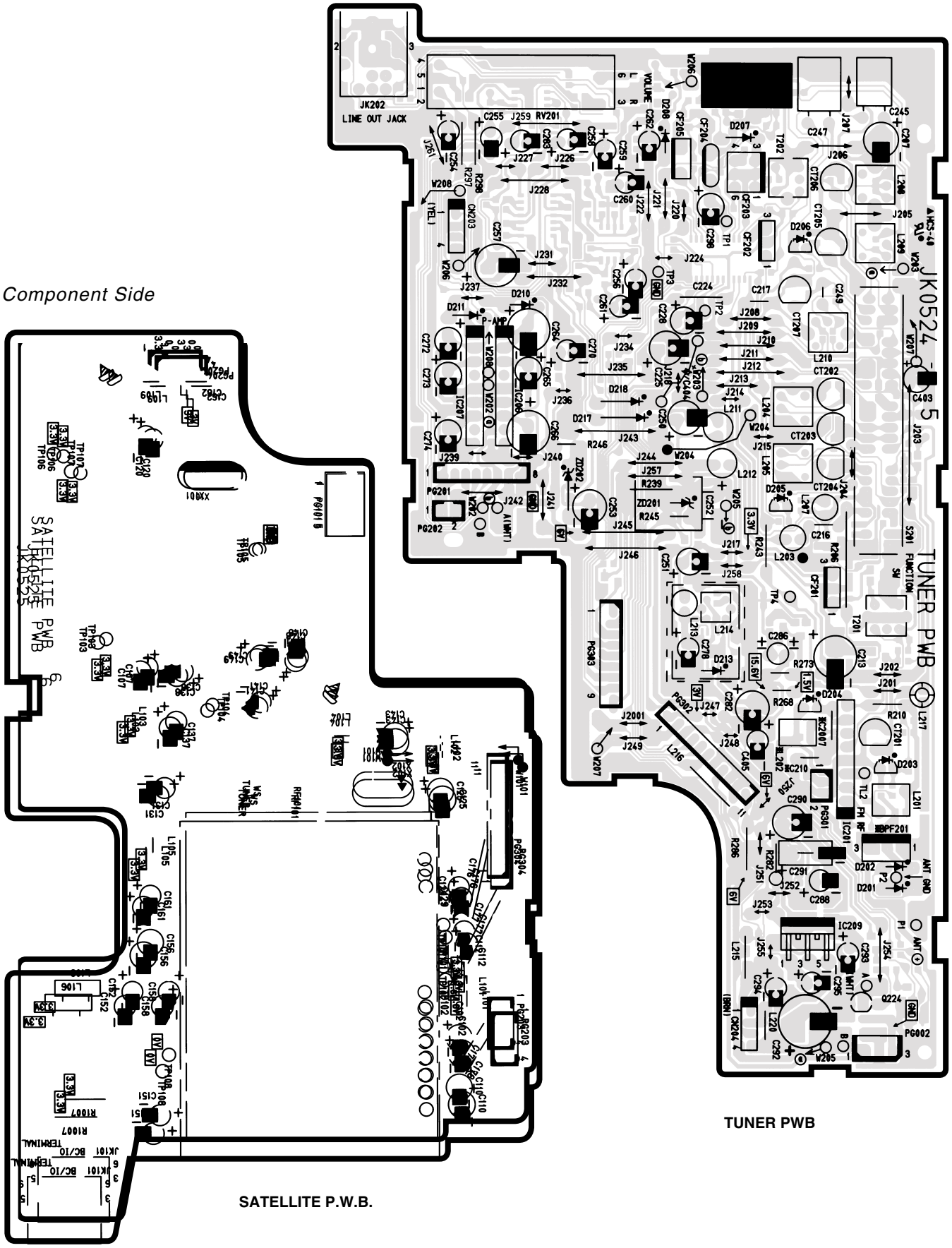
SATELLITE P.W.B.

Soldering Side

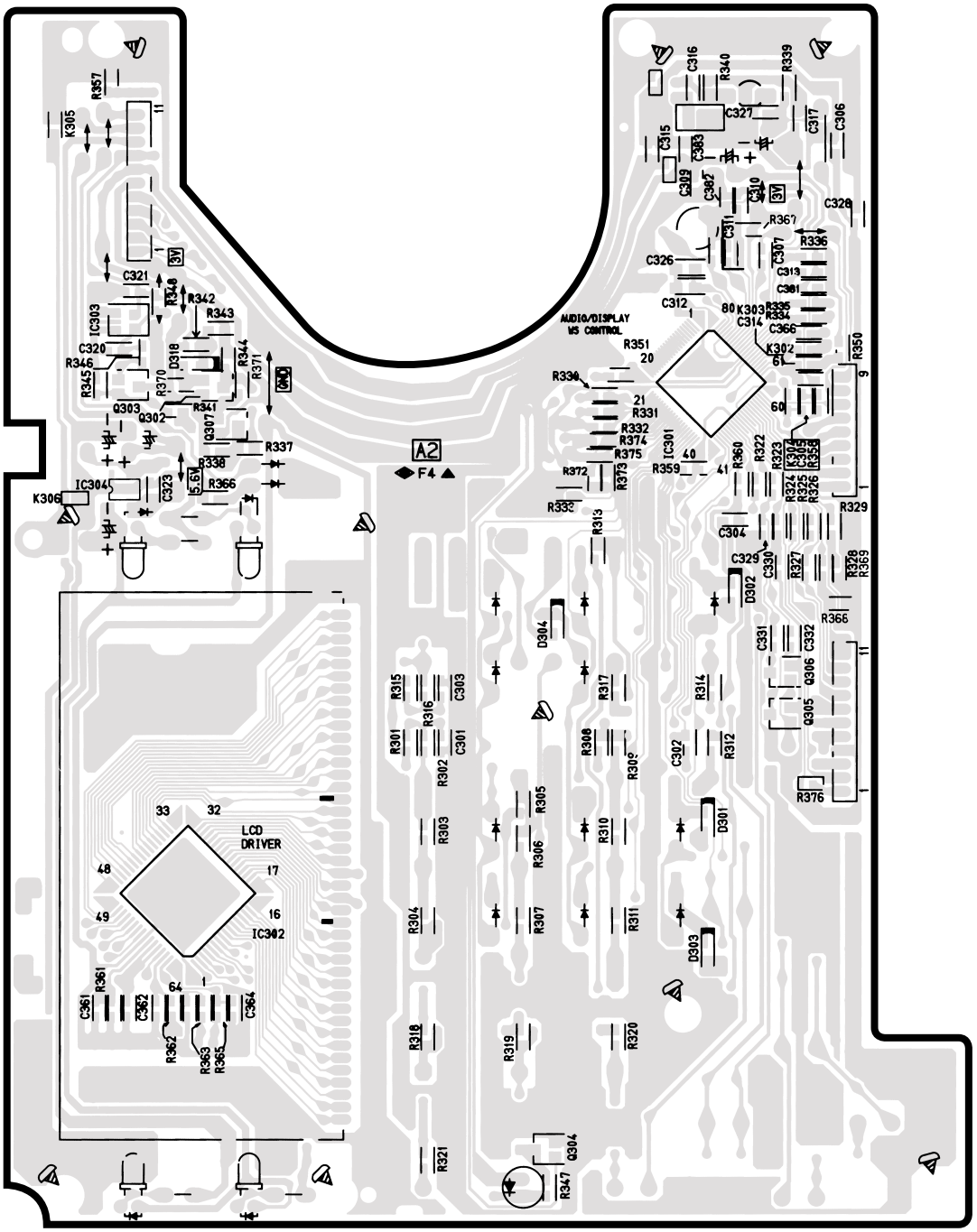


TUNER PWB

Component Side

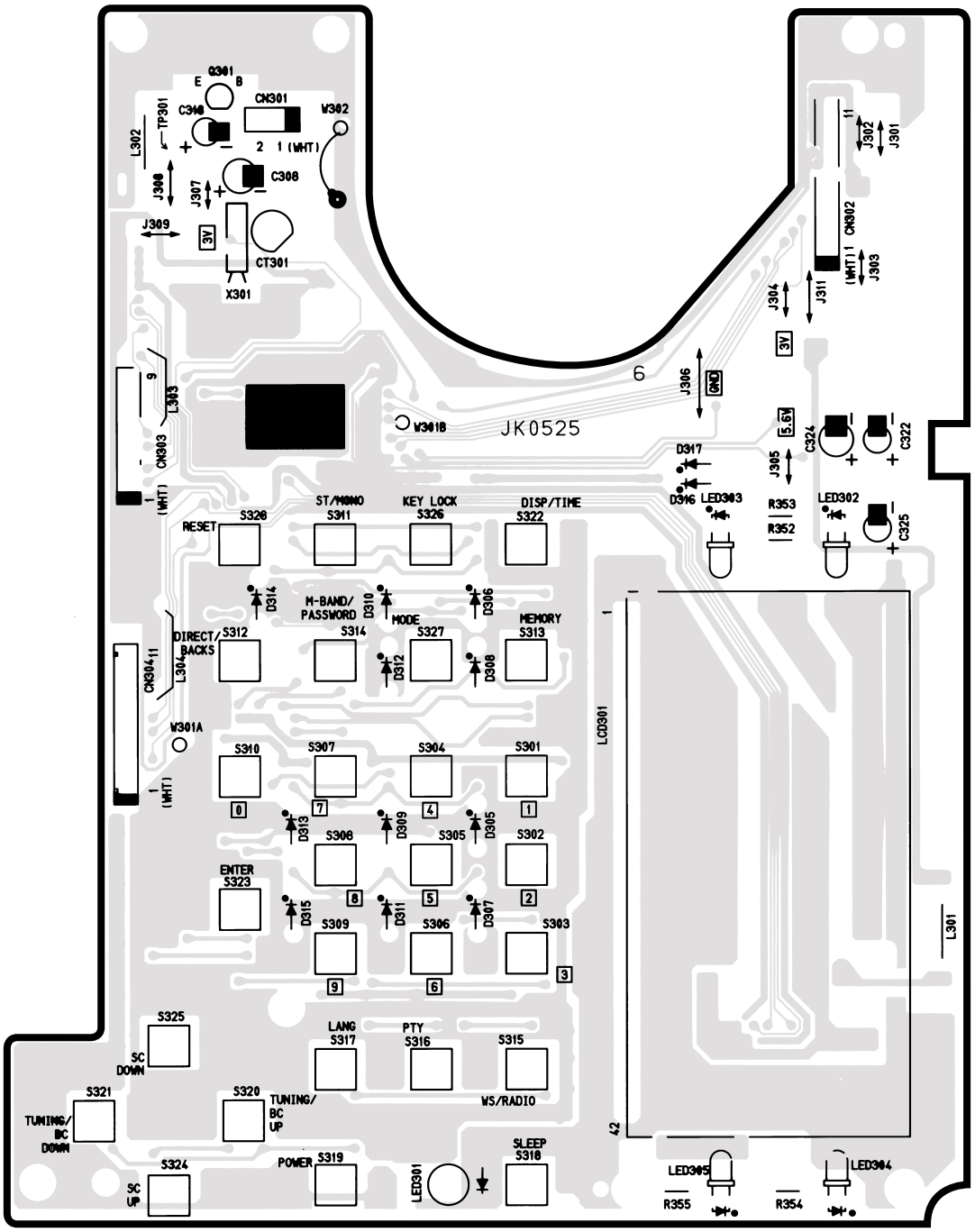


Soldering Side



MAIN PWB

Component Side

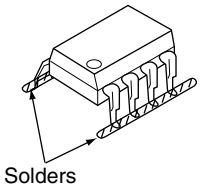


MAIN P.W.B.

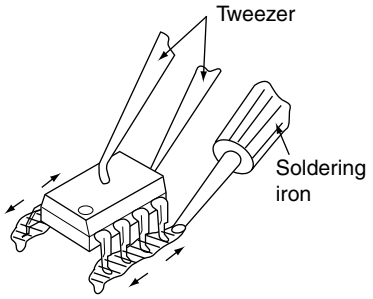
METHOD OF REMOVED IC
IC24LC194 (IC107)

When you reuse a replaced or removed IC, follow the next procedures.

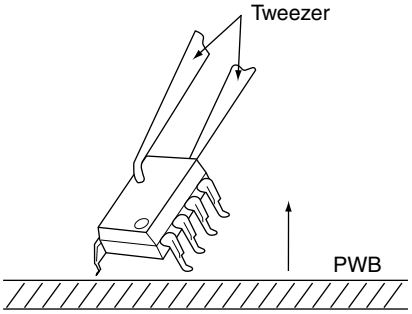
1. Solder pins on the IC more as shown in the illustration.



2. Melt the solders on the pins of both sides quickly using a soldering iron until the IC travels from the substrate. At the same time, have a tweezers on hand to pick up the IC.



3. Pick up and remove the IC with a tweezers slowly when it travels from the substrate. (Be careful not to delaminate the traces on the substrate.)



4. Remove and clean any redundant solders on traces on the substrate.

5. Remove the solders on leaders of the IC when you reuse it in the future.

CIRCUIT DIAGRAM

TUNER/DTS Circuit

CN302 Pin Voltages

Pin No.	1	2	3	4	5	6	7	8	9	10	11
WS	3	3	0	0	0	3	0	5.6	0	5.6	4.4
FM	3	0	3	0	0	3	0	6	0	6	4.8
MW	3	0	3	3	0	3	0	6	0	6	4.8
SW1	3	0	3	0	3	3	0	6	0	6	4.8
SW2	3	0	3	3	3	3	0	6	0	6	4.8

CN303 Pin Voltages

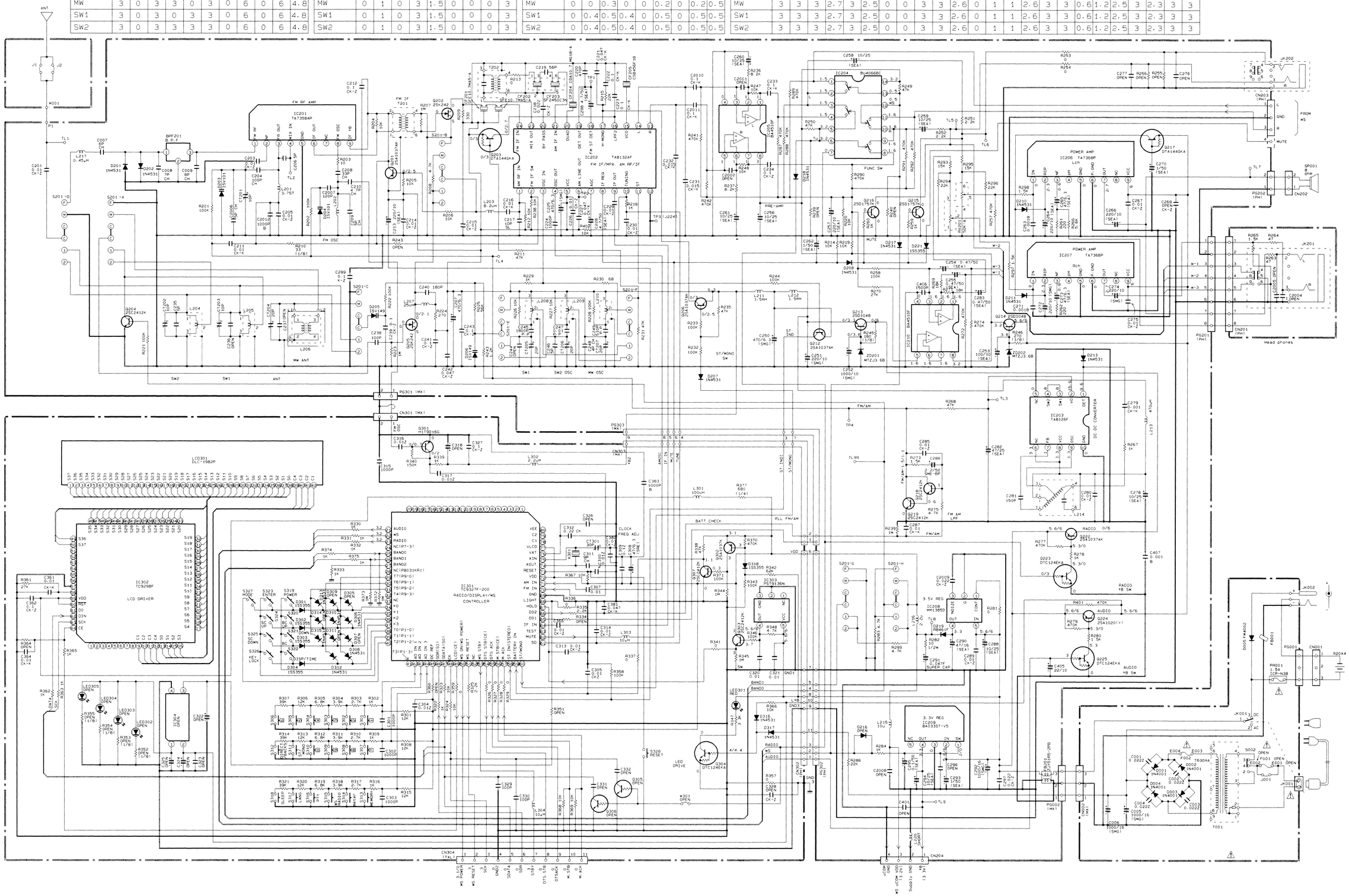
Pin No.	1	2	3	4	5	6	7	8	9
WS	0	1	0	3	0	0	0	0	0
FM	0	1	0	3	1.5	0	0	0	3
MW	0	1	0	3	1.5	0	0	0	3
SW1	0	1	0	3	1.5	0	0	0	3
SW2	0	1	0	3	1.5	0	0	0	3

IC201 Pin Voltages

Pin No.	1	2	3	4	5	6	7	8	9
FM	0.8	1.5	3	1.5	0	3	2.2	3	3
MW	0	0	0.3	0	0	0.2	0	0.2	0.5
SW1	0	0.4	0.5	0.4	0	0.5	0	0.5	0.5
SW2	0	0.4	0.5	0.4	0	0.5	0	0.5	0.5

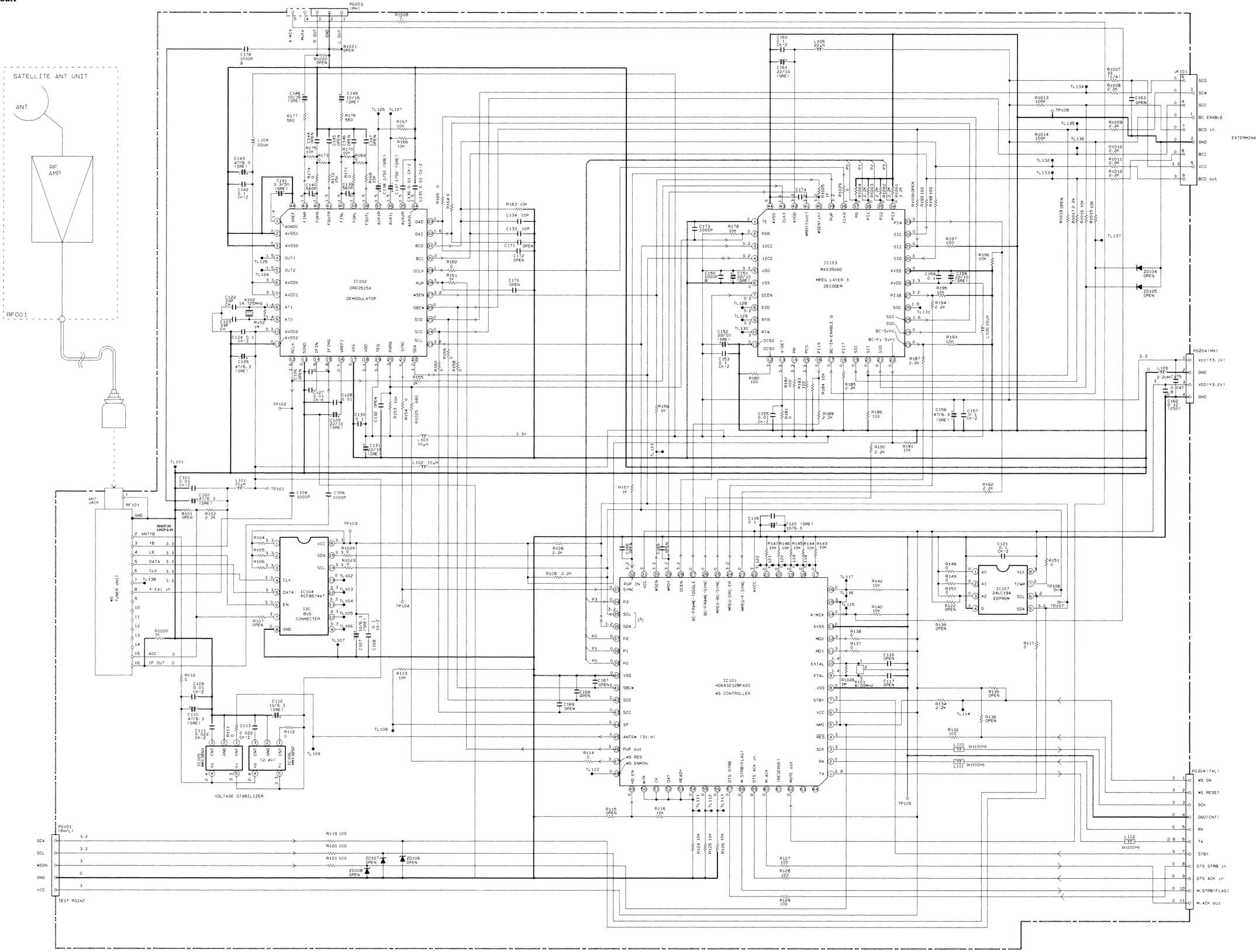
IC202 Pin Volages

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
FM	3	3	3	3	3	2.4	0.4	0	3	3	2.6	0	1	1	2.6	2.7	3	0.6	1	2.2	3	2.8	3	3
MW	3	3	3	2.7	3	2.5	0	0	3	3	2.6	0	1	1	2.6	3	3	0.6	1.2	2.5	3	2.3	3	3
SW1	3	3	3	2.7	3	2.5	0	0	3	3	2.6	0	1	1	2.6	3	3	0.6	1.2	2.5	3	2.3	3	3
SW2	3	3	3	2.7	3	2.5	0	0	3	3	2.6	0	1	1	2.6	3	3	0.6	1.2	2.5	3	2.3	3	3

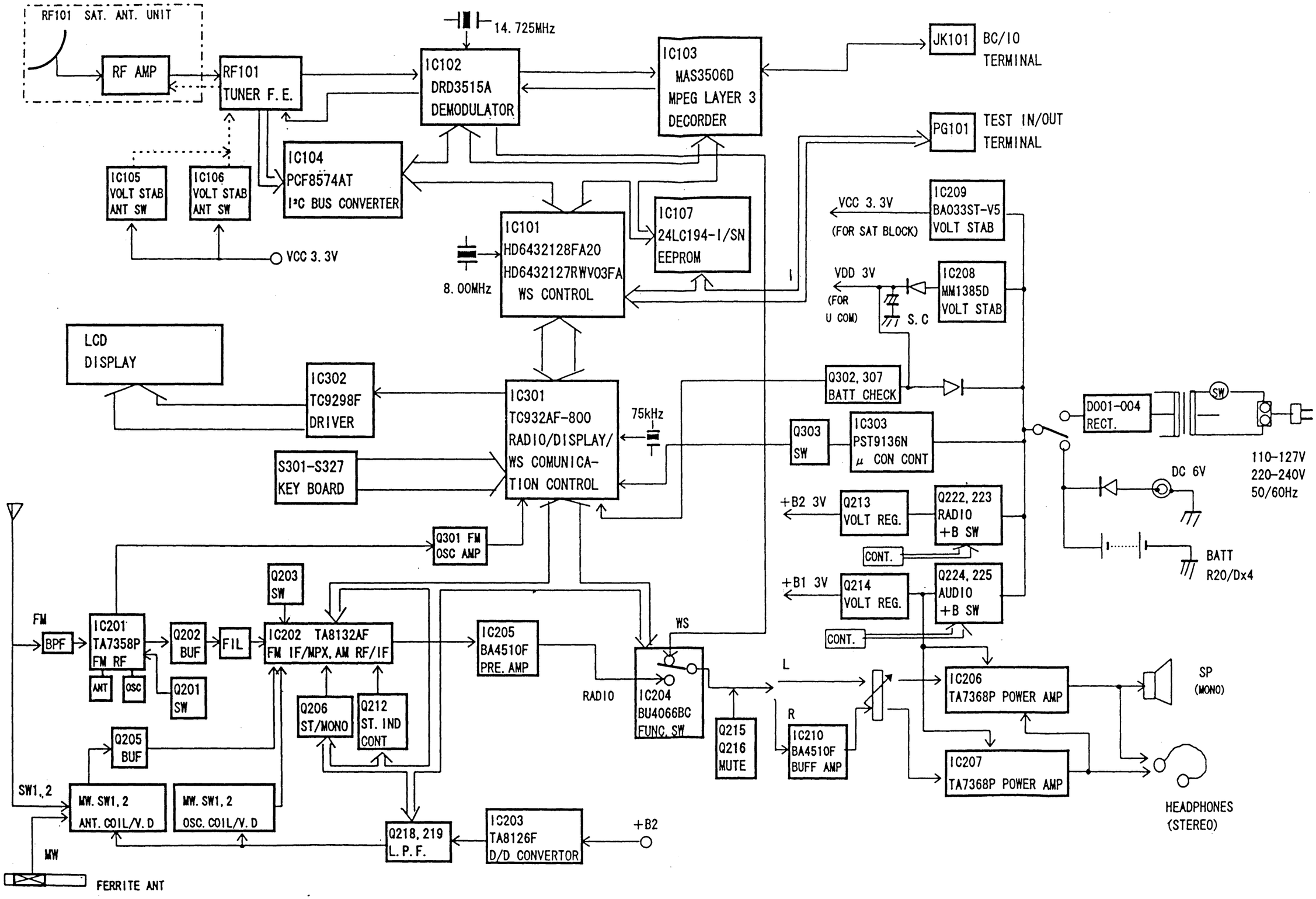


CIRCUIT DIAGRAM

SATELLITE Circuit



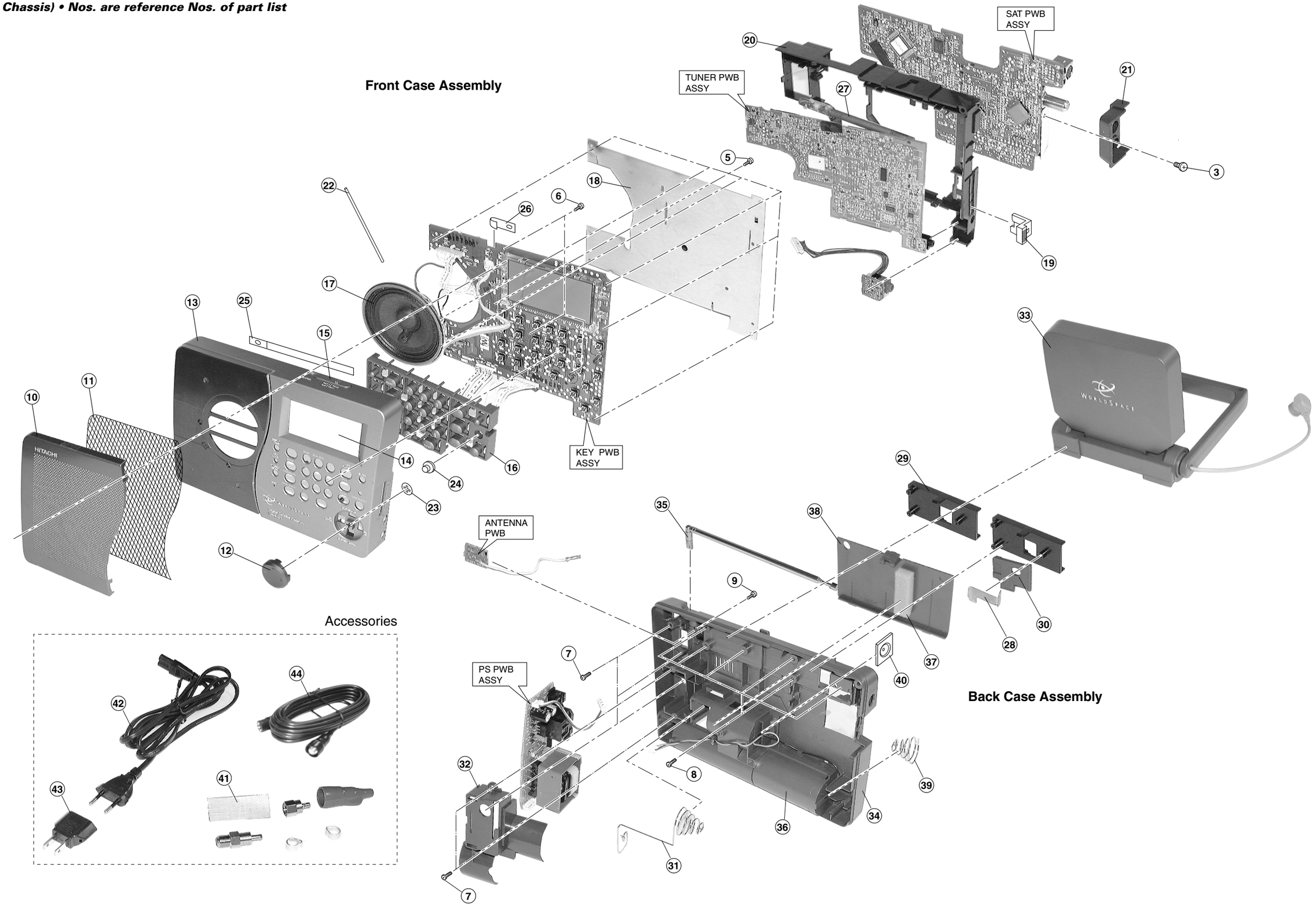
BLOCK DIAGRAM



EXPLODED VIEW

(Cabinet Chassis) • Nos. are reference Nos. of part list

Front Case Assembly



Accessories

Back Case Assembly

THE UPDATED PARTS LIST

FOR THIS MODEL IS

AVAILABLE ON ESTA

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International Sales Division
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